HI-1567, HI-1568

MIL-STD-1553 / 1760
5V Monolithic Dual Transceivers

November 2017

DESCRIPTION

The HI-1567 and HI-1568 are low power CMOS dual transceivers designed to meet the requirements of MIL-STD-1553 and MIL-STD-1760 specifications.

The transmitter section of each bus takes complementary CMOS / TTL Manchester II bi-phase data and converts it to differential voltages suitable for driving the bus isolation transformer. Separate transmitter inhibit control signals are provided for each transmitter.

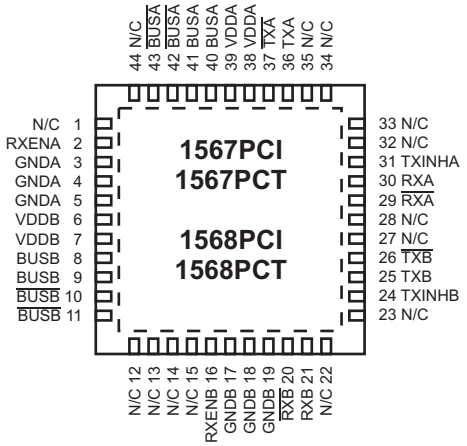
The receiver section of each bus converts the 1553 bus bi-phase data to complementary CMOS / TTL data suitable for input to a Manchester decoder. Each receiver has a separate enable input which can be used to force the output of the receiver to a logic 0 (HI-1567) or logic 1 (HI-1568).

To minimize the package size for this function, the transmitter outputs are internally connected to the receiver inputs, so that only two pins are required for connection to each coupling transformer.

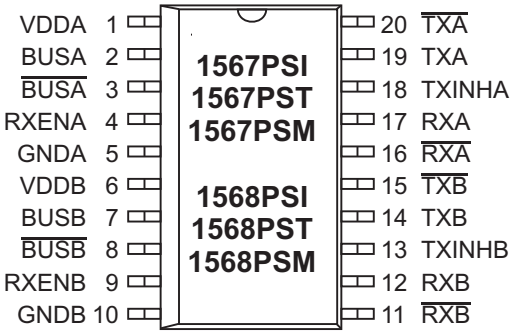
FEATURES

- Compliant to MIL-STD-1553A & B, MIL-STD-1760, ARINC 708A
- CMOS technology for low standby power
- Smallest footprint available in 44-pin plastic chip-scale package with integral heatsink
- Less than 1.0W maximum power dissipation
- Also available in DIP and small outline (ESOIC) package options
- Industrial and extended temperature ranges
- Industry standard pin configurations

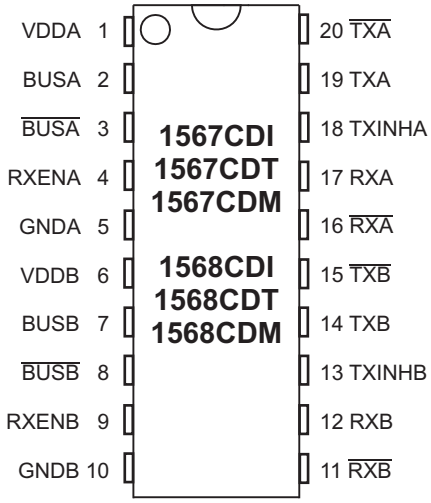
PIN CONFIGURATIONS



44 Pin Plastic 7mm x 7mm Chip-scale package



20 Pin Plastic ESOIC - WB package



20 Pin Ceramic DIP package

PIN DESCRIPTIONS

PIN (DIP/ESOIC)	SYMBOL	FUNCTION	DESCRIPTION
1	VDDA	power supply	+5 volt power for bus A
2	BUSA	analog	MIL-STD-1533 bus driver A, positive signal
3	$\overline{\text{BUSA}}$	analog	MIL-STD-1553 bus driver A, negative signal
4	RXENA	digital input	Receiver A enable. If low, forces RXA and $\overline{\text{RXA}}$ low (HI-1567) or High (HI-1568)
5	GNDA	power supply	Ground for bus A
6	VDDB	power supply	+5 volt power for bus B
7	BUSB	analog	MIL-STD-1533 bus driver B, positive signal
8	$\overline{\text{BUSB}}$	analog	MIL-STD-1553 bus driver B, negative signal
9	RXENB	digital input	Receiver B enable. If low, forces RXB and $\overline{\text{RXB}}$ low (HI-1567) or High (HI-1568)
10	GNDB	power supply	Ground for bus B
11	$\overline{\text{RXB}}$	digital output	Receiver B output, inverted
12	RXB	digital output	Receiver B output, non-inverted
13	TXINHB	digital input	Transmit inhibit, bus B. If high BUSB, $\overline{\text{BUSB}}$ disabled
14	TXB	digital input	Transmitter B digital data input, non-inverted
15	$\overline{\text{TXB}}$	digital input	Transmitter B digital data input, inverted
16	$\overline{\text{RXA}}$	digital output	Receiver A output, inverted
17	RXA	digital output	Receiver A output, non-inverted
18	TXINHA	digital input	Transmit inhibit, bus A. If high BUSA, $\overline{\text{BUSA}}$ disabled
19	TXA	digital input	Transmitter A digital data input, non-inverted
20	$\overline{\text{TXA}}$	digital input	Transmitter A digital data input, inverted

FUNCTIONAL DESCRIPTION

The HI-1567 family of data bus transceivers contains differential voltage source drivers and differential receivers. It is intended for applications using a MIL-STD-1553 A/B data bus. The device produces a trapezoidal output waveform during transmission.

TRANSMITTER

Data input to the device's transmitter section is from the complementary CMOS /TTL inputs TXA/B and $\overline{\text{TXA}}$/$\overline{\text{B}}$. The transmitter accepts Manchester II bi-phase data and converts it to differential voltages on BUSA/B and $\overline{\text{BUSA}}$/$\overline{\text{B}}$. The transceiver outputs are either direct- or transformer-coupled to the MIL-STD-1553 data bus. Both coupling methods produce a nominal voltage on the bus of 7.5 volts peak to peak.

The transmitter is automatically inhibited and placed in the high impedance state when both TXA/B and $\overline{\text{TXA}}$/$\overline{\text{B}}$ are driven with the same logic state. A logic "1" applied to the TXINHA/B input forces the transmitter to the high impedance state, regardless of the state of TXA/B and $\overline{\text{TXA}}$/$\overline{\text{B}}$.

RECEIVER

The receiver accepts bi-phase differential data from the MIL-STD-1553 bus through the same direct- or transformer-coupled interface as the transmitter. The receiver's differential input stage drives a filter and threshold comparator that produces CMOS/TTL data at the RXA/B and $\overline{\text{RXA}}$/$\overline{\text{B}}$ output pins. When the MIL-STD-1553 bus is idle and RXENA or RXENB are high, RXA/B will be logic "0" on HI-1567 and logic "1" on HI-1568.

The receiver outputs are forced to the bus idle state (logic "0" for HI-1567 or logic "1" for HI-1568) when RXENA or RXENB is low.

MIL-STD-1553 BUS INTERFACE

A direct-coupled interface (see Figure 2) uses a 1:2.5 ratio isolation transformer and two 55 ohm isolation resistors between the transformer and the bus. The primary center-tap of the isolation transformer must be connected to GND.

In a transformer-coupled interface (see Figure 2), the transceiver is connected to a 1:1.79 isolation transformer which in turn is connected to a 1:1.4 coupling transformer. The transformer coupled method also requires two coupling resistors equal to 75% of the bus characteristic impedence (Zo) between the coupling transformer and the bus.

Figure 3 and Figure 4 show test circuits for measuring electrical characteristics of both direct- and transformer-coupled interfaces respectively. (See electrical characteristics on the following pages).

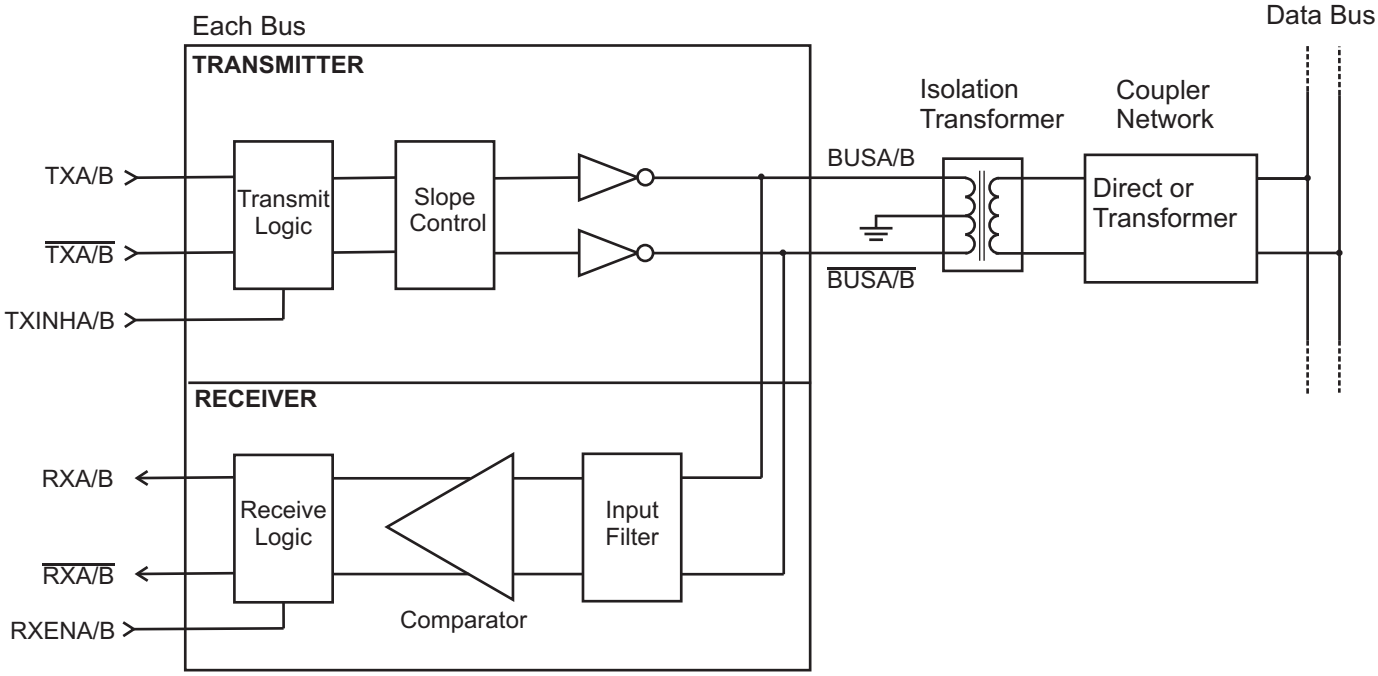
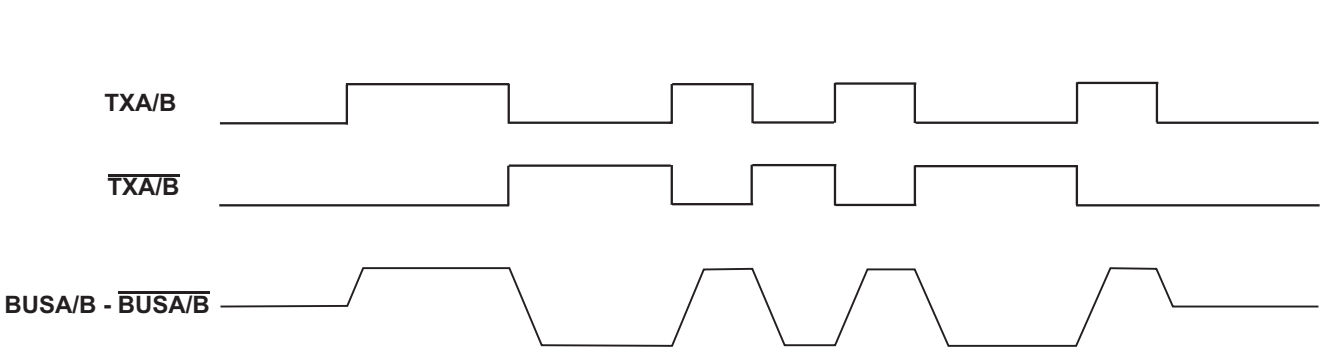
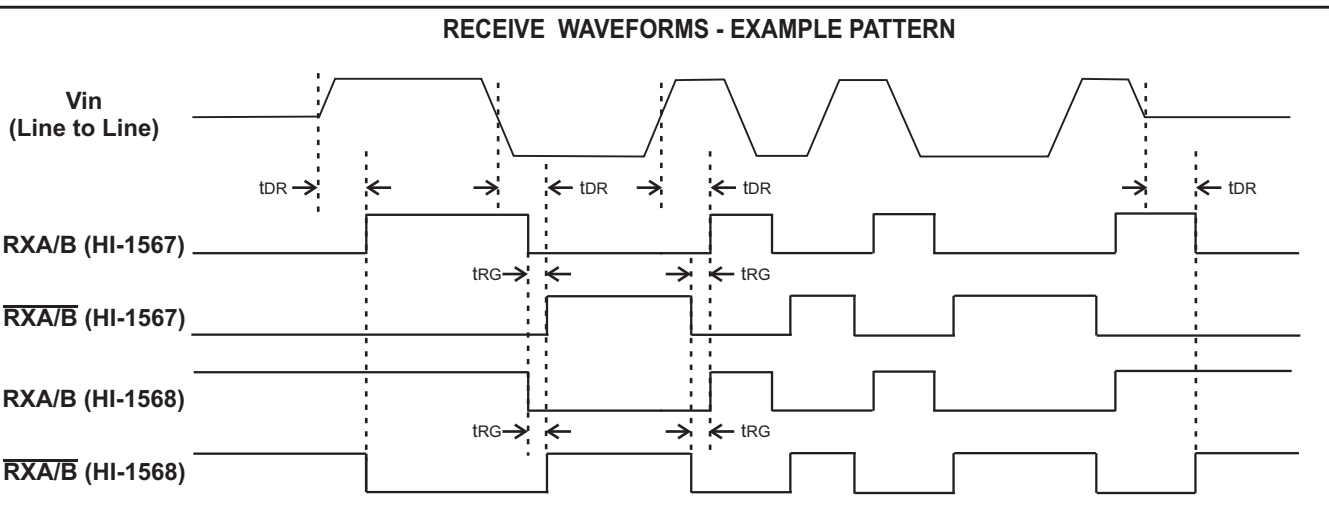


Figure 1. Block Diagram





ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD)	-0.3 V to +7 V
Logic input voltage range	-0.3 V dc to +5.5 V
Receiver differential voltage	50 Vp-p
Driver peak output current	+1.0 A
Solder reflow Temperature	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage

VDD..... 5V... ±5%

Temperature Range

Industrial .....-40°C to +85°C
Extended.....-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

VDD = 5.0V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	VDD		4.75	5	5.25	V
Total Supply Current	ICC1	Not Transmitting		14	22	mA
	ICC2	Transmit one bus @ 50% duty cycle		200	340	mA
	ICC3	Transmit one bus @ 100% duty cycle		400	550	mA
Power Dissipation	PD1	Not Transmitting			0.11	W
	PD2	Transmit one bus @ 100% duty cycle		0.70	0.95	W
Min. Input Voltage (HI)	V_{IH}	Digital inputs	2.0	1.4		V
Max. Input Voltage (LO)	V_{IL}	Digital inputs		1.4	0.8	V
Min. Input Current (HI)	I_{IH}	V_{IH} = 4.9V, Digital inputs			20	µA
Max. Input Current (LO)	I_{IL}	V_{IL} = 0.1V, Digital inputs	-20			µA
Min. Output Voltage (HI)	V_{OH}	I_{OUT} = -0.4mA, Digital outputs	2.7			V
Max. Output Voltage (LO)	V_{OL}	I_{OUT} = 4.0mA, Digital outputs			0.4	V
RECEIVER (Measured at Point "A_D" in Figure 3 unless otherwise specified)						
Input resistance	R_{IN}	Differential (at chip pins)	20			Kohm
Input capacitance	C_{IN}	Differential			5	pF
Common mode rejection ratio	CMRR		40			dB
Input common mode voltage	V_{ICM}		-5.0		5.0	V-pk
Threshold Voltage - Direct-coupled Detect	V_{THD}	1 Mhz Sine Wave	1.15			Vp-p
		Measured at Point "A_D" in Figure 3 RXA/B, $\overline{RXA/B}$ pulse width >70ns				
No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.28	Vp-p
Threshold Voltage - Transformer-coupled Detect	V_{THD}	1 Mhz Sine Wave Measured at Point "A_T" in Figure 4 RXA/B, $\overline{RXA/B}$ pulse width >70ns	0.86			Vp-p
No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.20	Vp-p

DC ELECTRICAL CHARACTERISTICS (cont.)

VDD = 5.0V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
TRANSMITTER (Measured at Point "AD" in Figure 3 unless otherwise specified)						
Output Voltage Direct coupled	VOUT	35 ohm load (Measured at Point "AD" in Figure 3)	7.0		9.0	Vp-p
Output Voltage Transformer coupled	VOUT	70 ohm load (Measured at Point "AT" in Figure 4)	20.0		27.0	Vp-p
Output Noise	VON	Differential, inhibited			10.0	mVp-p
Output Dynamic Offset Voltage Direct coupled	VDYN	35 ohm load (Measured at Point "AD" in Figure 3)	-90		90	mV
Output Dynamic Offset Voltage Transformer coupled	VDYN	70 ohm load (Measured at Point "AT" in Figure 4)	-250		250	mV
Output resistance	ROUT	Differential, not transmitting	10			Kohm
Output Capacitance	COUT	1 MHz sine wave			15	pF

AC ELECTRICAL CHARACTERISTICS

VDD = 5.0V, GND = 0V, T_A =Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER (Measured at Point "AT" in Figure 4)						
Receiver Delay	tDR	From input zero crossing to RXA/B or $\overline{RXA/B}$			450 Note 3	ns
Receiver gap time	tRG	Spacing between RXA/B and $\overline{RXA/B}$ pulses	90 Note 1		365 Note 2	ns
Receiver Enable Delay	tREN	From RXENA/B rising or falling edge to RXA/B or $\overline{RXA/B}$			40	ns
TRANSMITTER (Measured at Point "AD" in Figure 3)						
Driver Delay	tDT	TXA/B, $\overline{TXA/B}$ to BUSA/B, $\overline{BUSA/B}$			150	ns
Rise time	tr	35 ohm load	100		300	ns
Fall Time	tf	35 ohm load	100		300	ns
Inhibit Delay	tDI-H	Inhibited output			100	ns
	tDI-L	Active output			150	ns

Note 1. Measured using a 1 MHz sinusoid, 20 V peak to peak, line to line at point "AT" (Guaranteed but not tested).

Note 2. Measured using a 1 MHz sinusoid, 860 mV peak to peak, line to line at point "AT" (100% tested).

Note 3. Measured using a 1 MHz sinusoid, 860 mV peak to peak, line to line at point "AT". Measured from input zero crossing point.

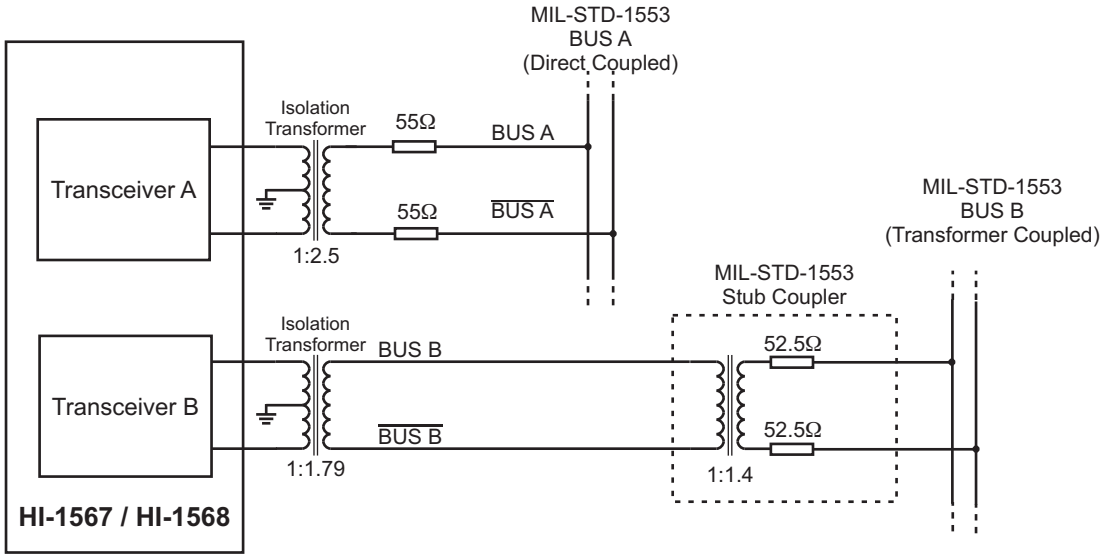


Figure 2. Bus Connection Example using HI-1567 or HI-1568

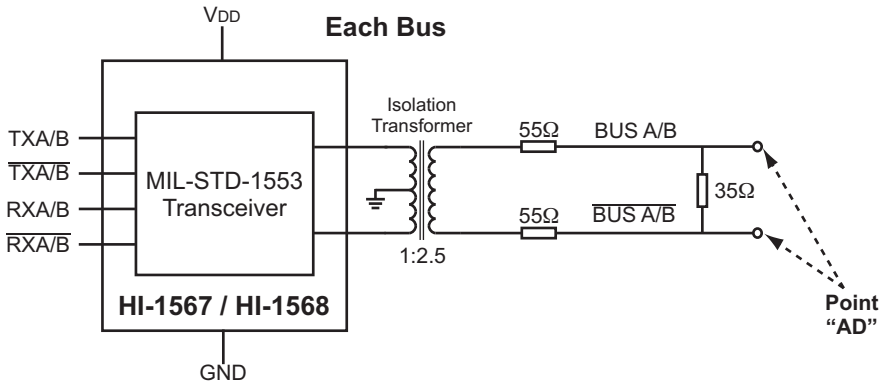


Figure 3. Direct Coupled Test Circuit

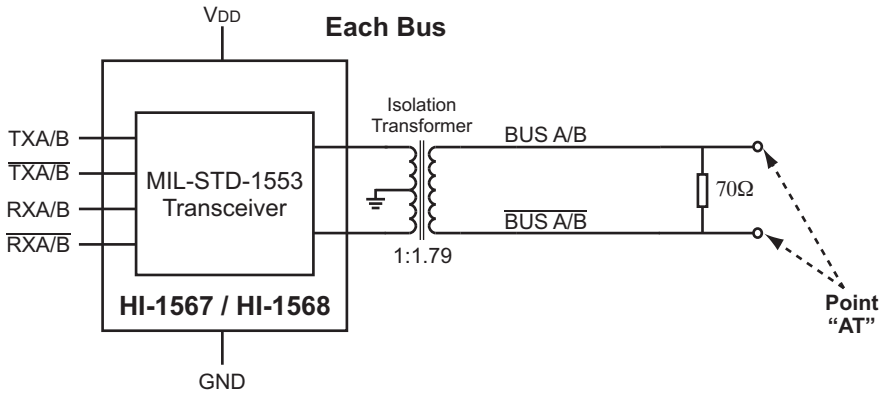


Figure 4. Transformer Coupled Test Circuit

HEAT SINK - ESOIC & CHIP-SCALE PACKAGE

Both the HI-1567PSI/T/M and HI-1568PSI/T/M use a 20-pin thermally enhanced SOIC package. The HI-1567PCI/T and HI-1568PCI/T use a plastic chip-scale package. These packages include a metal heat sink located on the bottom surface of the device. This heat sink should be soldered down to the printed circuit board for optimum thermal dissipation. The heat sink is electrically isolated and may be soldered to any convenient power or ground plane.

APPLICATIONS NOTE

Holt Applications Note AN-500 provides circuit design notes regarding the use of Holt's family of MIL-STD-1553 transceivers. Layout considerations, as well as recommended interface and protection components are included.

ORDERING INFORMATION

HI - 156x xx x x (Plastic)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
PC	44 PIN PLASTIC CHIP-SCALE LPCC (44PCS) not available with 'M' flow
PS	20 PIN PLASTIC ESOIC (Thermally Enhanced Wide SOIC w/Heat Sink, 20HWE)

PART NUMBER	RXENA = 0		RXENB = 0	
	RXA	$\overline{RXA}$	RXB	$\overline{RXB}$
1567	0	0	0	0
1568	1	1	1	1

HI - 156xCD x (Ceramic)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
I	-40°C TO +85°C	I	NO	Gold (Pb-free, RoHS compliant)
T	-55°C TO +125°C	T	NO	Gold (Pb-free, RoHS compliant)
M	-55°C TO +125°C	M	YES	Tin / Lead (Sn / Pb) Solder

PART NUMBER	RXENA = 0		RXENB = 0		PACKAGE DESCRIPTION
	RXA	$\overline{RXA}$	RXB	$\overline{RXB}$	
1567CD	0	0	0	0	20 PIN CERAMIC SIDE BRAZED DIP (20C)
1568CD	1	1	1	1	20 PIN CERAMIC SIDE BRAZED DIP (20C)

RECOMMENDED TRANSFORMERS

The HI-1567 and HI-1568 transceivers have been characterized for compliance with the electrical requirements of MIL-STD-1553 when used with the following transformers. Holt recommends the Premier Magnetics parts as offering the best combination of electrical performance, low cost and small footprint.

MANUFACTURER	PART NUMBER	APPLICATION	TURNS RATIO(S)	DIMENSIONS
Premier Magnetics	PM-DB2725EX	Isolation	Dual ratio 1:1.79, 1:2.5	0.4 x 0.4 x 0.242 inches
Premier Magnetics	PM-DB2702	Stub coupling	1:1.4	.625 x .625 x .250 inches
Premier Magnetics	PM-DB-2791S	Isolation	1:2.5	0.4 x 0.4 x 0.185 inches
Premier Magnetics	PM-DB-2795S	Isolation	1:1.79	0.4 x 0.4 x 0.185 inches
Premier Magnetics	PM-DB-2798S	Isolation	Dual ratio 1:1.79, 1:2.5	0.4 x 0.4 x 0.185 inches
Premier Magnetics	PM-DB-2762	Isolation	Dual core 1:2.5	0.4 x 0.4 x 0.320 inches
Premier Magnetics	PM-DB-2766	Isolation	Dual core 1:1.79	0.4 x 0.4 x 0.320 inches

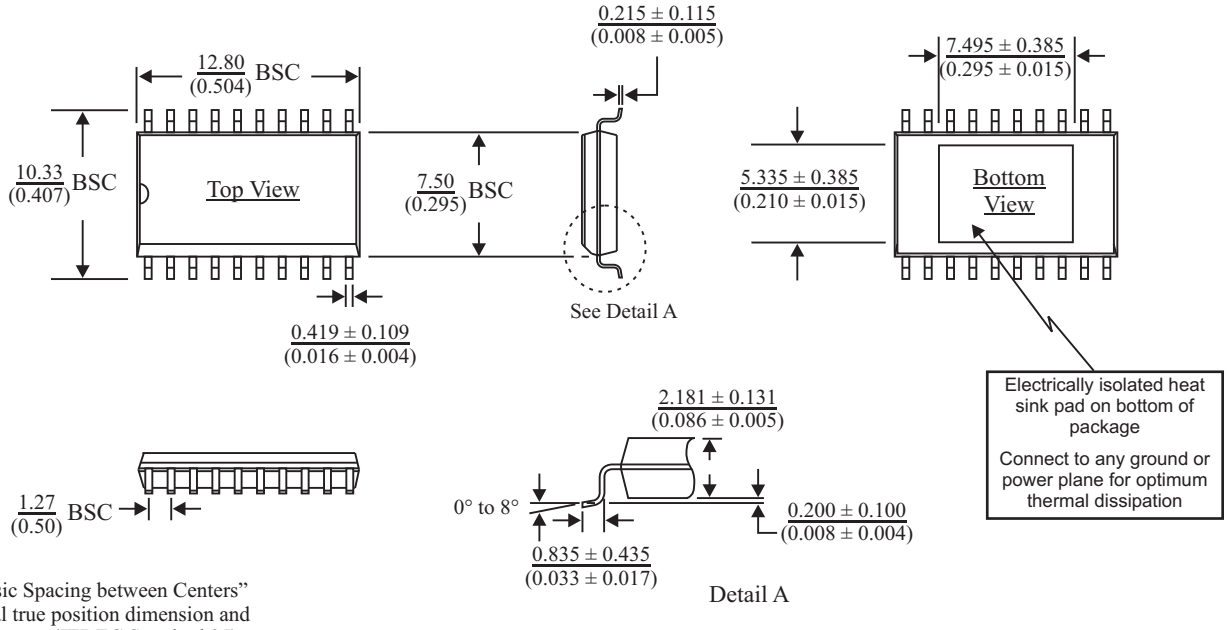
REVISION HISTORY

Document	Rev.	Date	Description of Change
DS1567	O	09/26/08	Clarification of transmitter and receiver functions in Description, clarified available temperature ranges, and corrected a dimension in Recommended Transformers table.
	P	07/24/09	Corrected typographical errors in package dimensions.
	Q	07/15/13	Updated functional description for clarity. Revised figures 2, 3 and 4. Updated package drawings.
	R	05/21/14	Updated Figure 2 and package drawings.
	S	05/26/15	Clarified t_{RG} test conditions in AC Characteristics Table. Corrected bus labeling on Tables 2 and 3. Updated Recommended Transformers table.
	T	07/28/16	Added “Point AD” to Pg. 6 Figure. 3.
	U	11/30/17	Correct typo in DC Electrical Characteristics Table; VOL incorrectly labeled as VIH. Remove Power Dissipation from Absolute Maximum Ratings Table. Remove Thermal Characteristics Table. Refer to website for thermal resistance data. Correct typo in Figure 2.

20-PIN PLASTIC SMALL OUTLINE (ESOIC) - WB
(Wide Body, Thermally Enhanced)

millimeters (inches)

Package Type: 20HWE

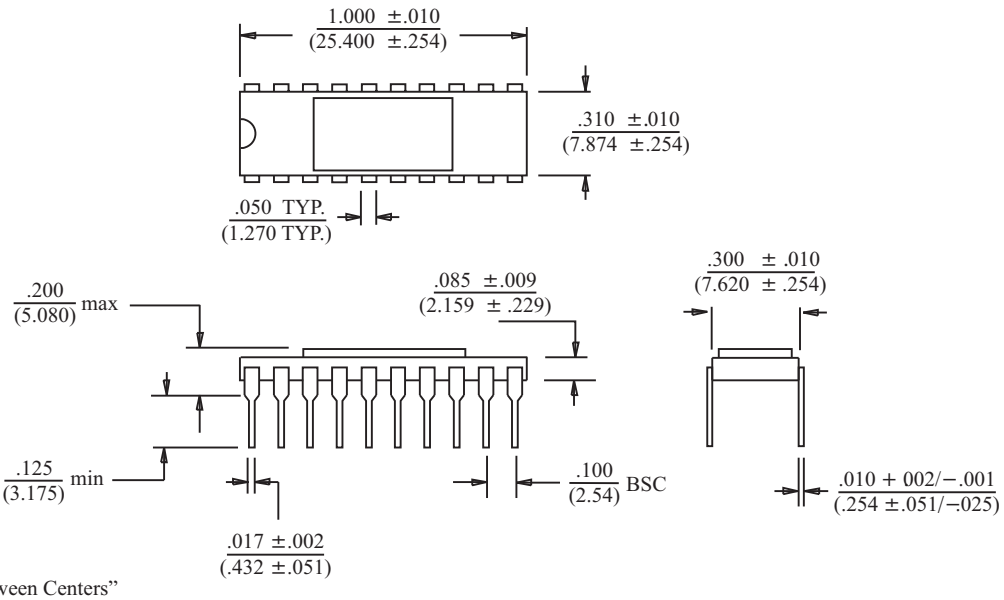


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

20-PIN CERAMIC SIDE-BRAZED DIP

inches (millimeters)

Package Type: 20C

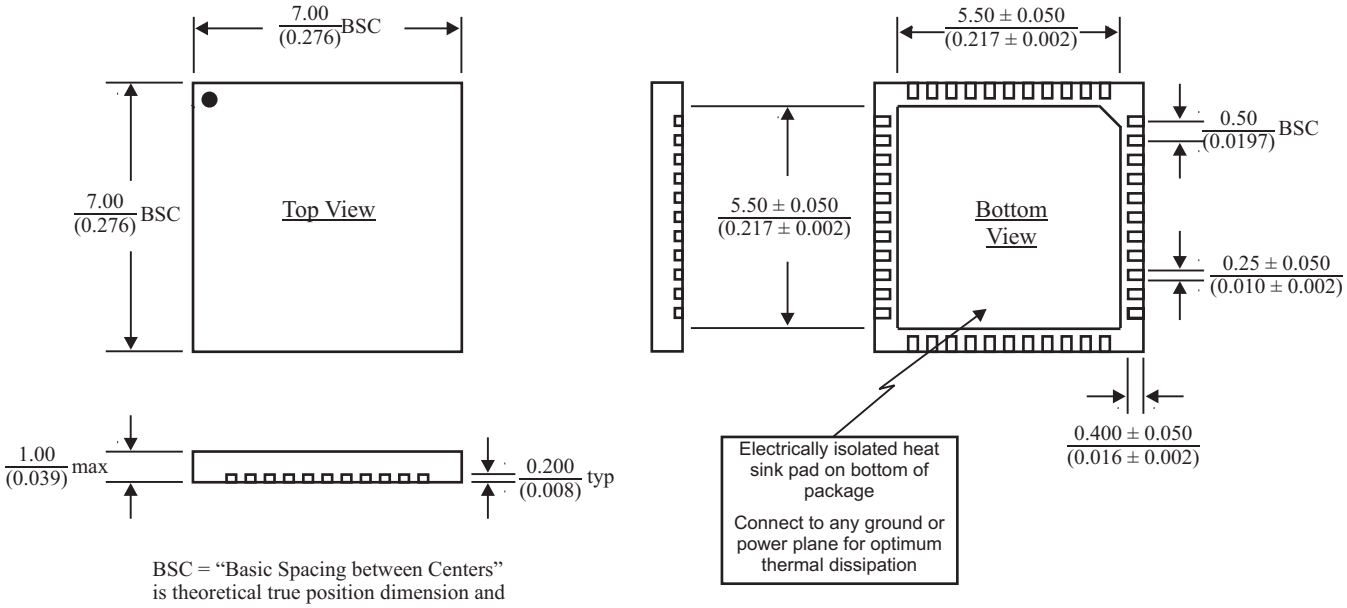


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 44PCS



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