HOLT INTEGRATED CIRCUITS INC.

AN-110

Using the HI-868X Interface Device for ARINC 561 Applications Note

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INTRODUCTION

ARINC 561 is a six wire system involving three separate twisted pairs. The three pairs serve as CLOCK, SYNC and DATA. The inputs are Non-Return-to-Zero (NRZ) logic with levels of +12V for a logic "1" and 0V for a logic "0" The CLOCK frequency is 11.5 ± 3.5 KHz and the data word length is 32 bits with no parity bit.

In order to use the HI-868X series of ARINC Interface devices for ARINC 561 the bus signals must be converted from +12V levels to +5V CMOS levels and the DATA translated to a Return-to-Zero (RZ) logic format.

This is easily accomplished by simple level translation of the CLOCK, SYNC and DATA signals to 5 volts and gating the resulting DATA with the translated CLOCK and SYNC signals. The gated DATA1 and DATA0 signals are connected directly to the INA and INB inputs of the HI-8683 as shown in Figures 1 & 2.

The Holt HI-8685 and HI-8686 receive ARINC 561 data in a similar manner through the Test inputs. In this case, the inverse of the DATA1 ($\overline{DATA1}$)is connected to the TESTB input and the inverse of DATA0 ($\overline{DATA0}$) is connected to the TESTA input as illustrated in Figures 3 & 4.

A GAP CLOCK frequency of 0.2 MHz is used to detect the beginning of an ARINC 561 word. PARITY ENB input must also be set low for proper data reception since there is no parity bit with this protocol.

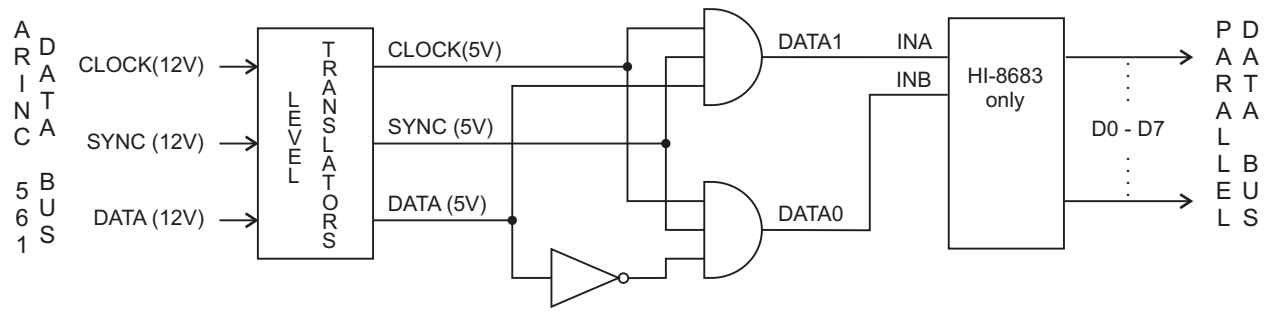

Figure 1 - Simplified Logic Diagram for HI-8683

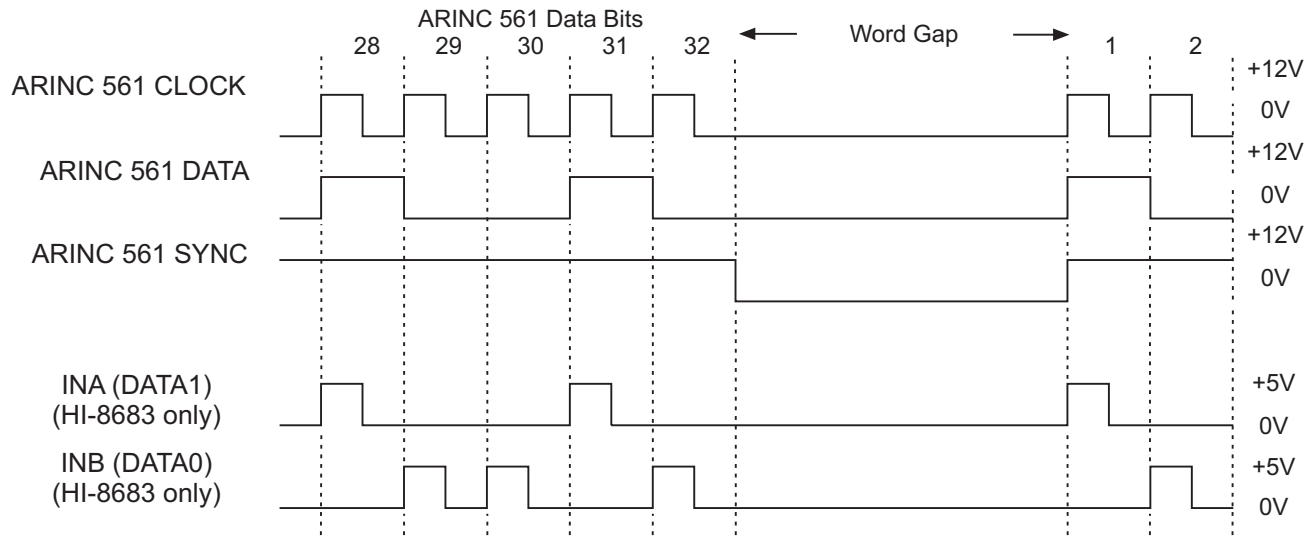

Figure 2 - Input Waveforms for HI-8683

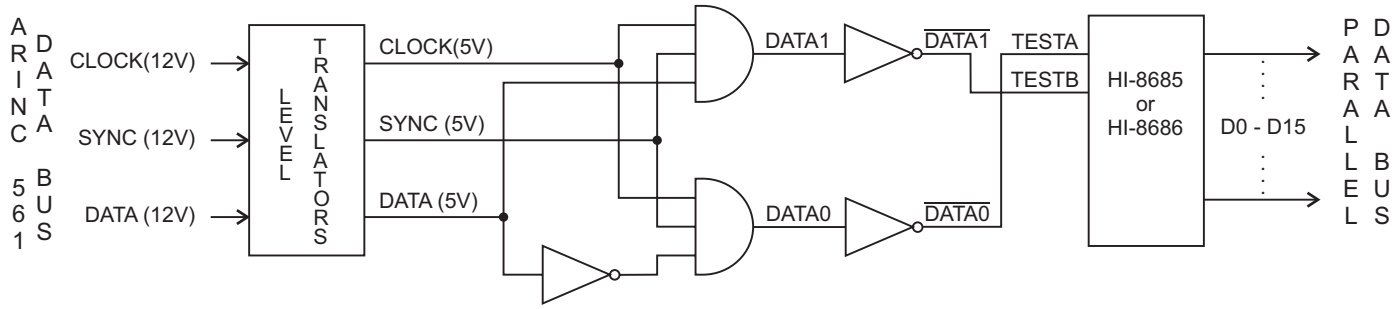

Figure 3 - Simplified Logic Diagram for HI-8685 and HI-8686

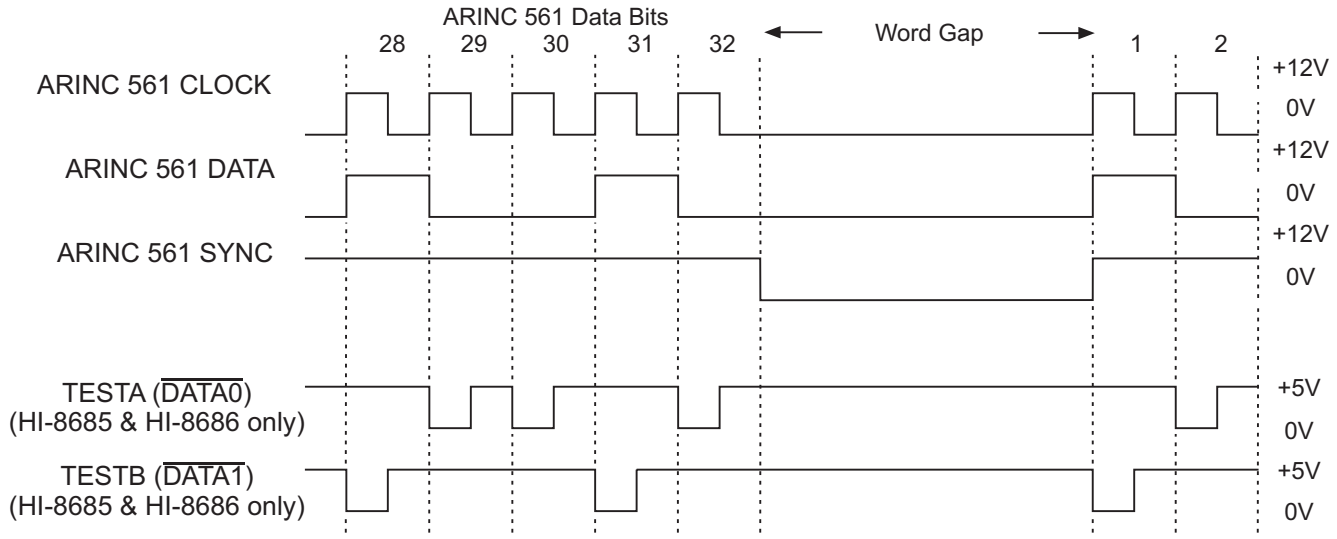

Figure 4 - Input Waveforms for HI-8685 and HI-8686