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Final

P11_0278_006_HI3110G_report_r00
Date of Approval: 2012-Jan-11

Test Report

Device Under Test		**Customer**	
Object	HI - 3110	Order No.	P11_0278
Manufacturer	Holt Integrated Circuits, Inc.	Name	Holt Integrated Circuits, Inc.
Type	HI - 3110 G	Address	23351 Madero Mission Viejo, CA 92691 USA
Serial number / version	G		

Number of Pages	59
Test Period	from 2011-Dec-12 until 2011-Dec-19
Test Method / Test Requirement	CAN Conformance Test
Performed Tests and References	1 ISO CAN Conformance Tests according to "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan" and C&S enhancement/ corrections according to "CAN CONFORMANCE TESTING Test Specification C&S Version 2.0 RC"
Conformance Test Results	The Test Results refer to the delivered device.
1 ISO CAN conformance tests (without test 8.7.9)	**PASS**

For detailed information see chapters Problem History and Test List at the following pages.

Approved by

Lothar Kukla, Project Manager

Test performed by

Andreas Meitrodt, Project Engineer

Table of Content

Revision History

Old revision	New revision	Amendment Description	Editor
–	d00	Initial version	AM
d00	R00	Final version	AM

1 Device Under Test (detailed)

General	
Manufacturer	Holt Integrated Circuits, Inc.
Sample Marking	G
Test performed with DUT no.	1

Device Specification	
Name	HI - 3110
Version	G
Design step	-
HW-Version	-
SW-Version	-

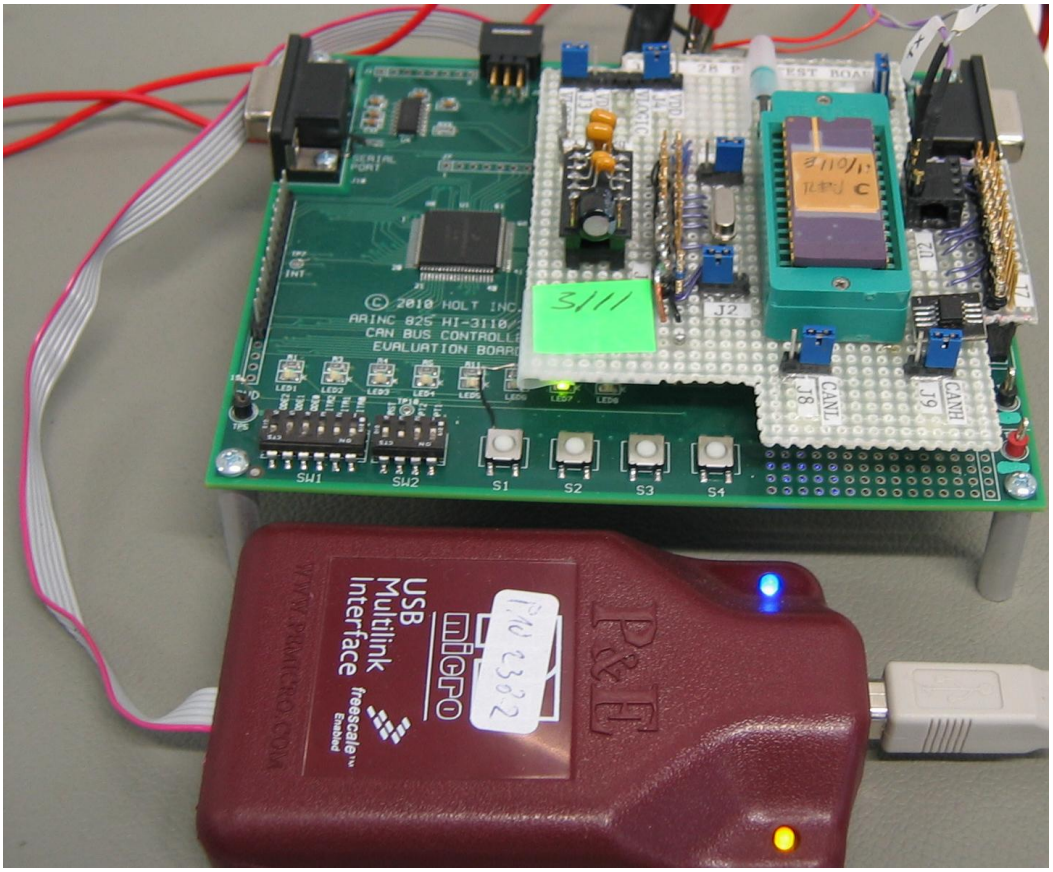
Documentation	
Hardware manual	DS3110 Rev.A (September 2011)
User manual / datasheet	AN-175 Rev.NEW (August 2011)

Device Classification	
Evaluation board version	ARINC 825 HI-3110/3111 CAN Bus evaluation board
Quartz / crystal oscillator with	24MHz
CAN clock (bit timing)	12MHz (tests at different baud rates, refer to page 42)
CAN clock (ISO16845)	12MHz (tests at 100K baud)

Software Specification	
Emulator version	-
IDE version	Code Warrior 5.9
Compiler version	Code Warrior 5.9
Flash tool version	Code Warrior 5.9
UT name	csgwfcl174
IP address	172.17.2.165
LT name	csgwfut207
IP address	172.17.2.207

2 Setup for Device Under Test

2.1 Connection Plan



Used Pin connection	
Pin name	**Pin No.**
TX	**TRX socket**
RX	**TRX socket**
GND	**TRX socket**
UT_P0	**--**
UT_P1	**--**

3 Test Equipment

The following test equipment and test system have been used.

No.	Component	Manufacturer	Version / Type	ID
1	C&S CAN Conformance Tester	C&S	V3.0.3	
Test System 4				
2	Logic Analyzer System	Agilent	16702B	700046
3	Pattern Generator	Agilent	16720A	700048
4	Logic Analyzer Card	Agilent	16716A	700057
5	Clock-Pod	Agilent	10460A	500007
6	Data-Pod	Agilent	10462A	500013
7	CAN Card	Vector	CANbordXL	600023
8	Coupler Box	C&S	Version 6.0	CSHW000059

4 Technical Correspondence

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5 Problem History

1 Remark description			
Test Case No.	3.7.5 Synchronisation for e < 0 and |e| > SJW 3.7.8 Synchronisation before information processing time		
Test Specification *(Title, Version)*	C&S_CAN_Conformance_TestSpec_r2.0_D07_RC.doc (ISO16845:2004, 8.7.5) (ISO16845:2004, 8.7.8)		
Protocol Specification *(Title, Version)*	ISO11898:2003		
Test Object ID *(serial no., sample marking, ….)*	HI-3110		
Proved by	AM	*Proved at*	
Observation in Short The IUT will drive dominant level earlier as expected.			

Test Case Description

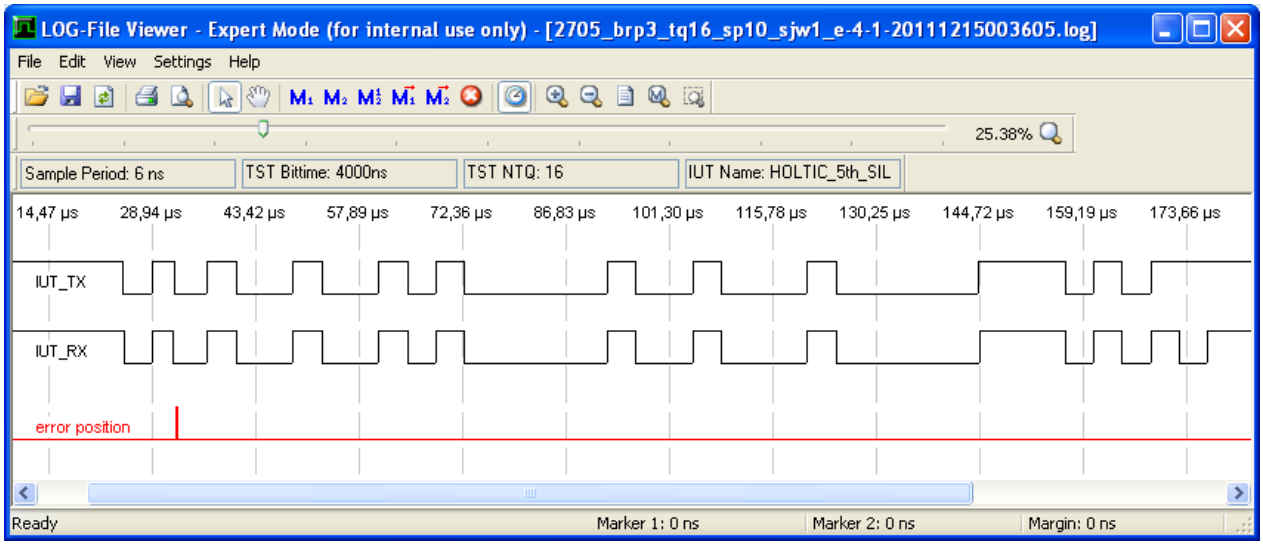
The IUT has to perform a soft synchronization as transmitter because an early recessive to dominant edge occur between sampling point and bit end. The following bit to transmit is dominant.

Remark Description

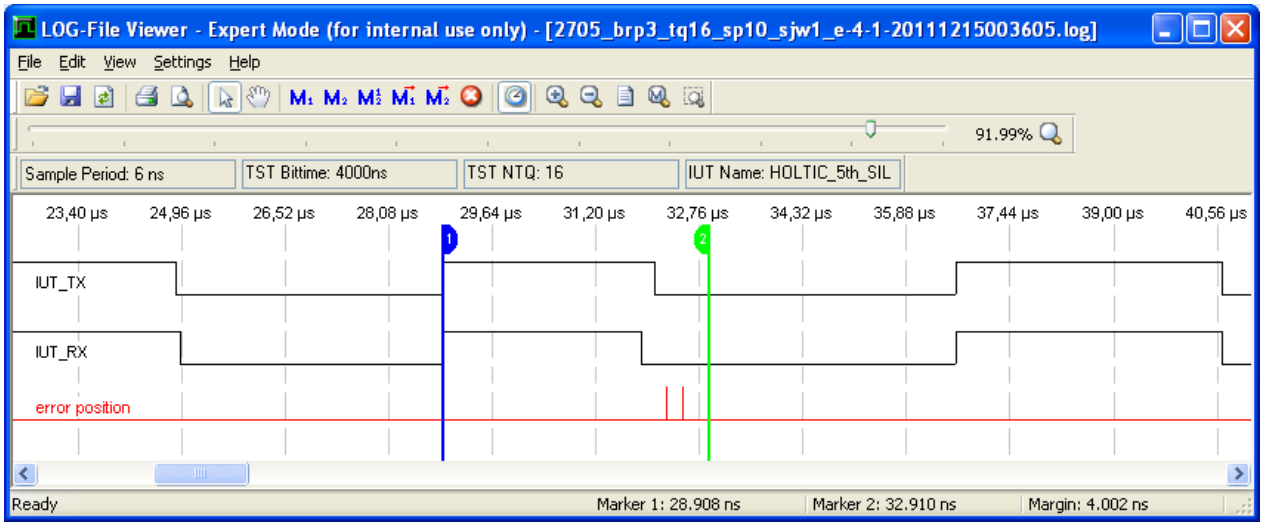
The IUT perform the soft synchronization correct. The IUT drive the TX output dominant after detection of the early edge. So the IUT driven dominant level overlay with the dominant level on IUT RX set by test system.

Visualization

Test sequence over all:



Detail:



The early edge on IUT RX is given between blue and green marker. The IUT TX line will “follow” one TQ later. The test system expect the IUT will drive the recessive bit level until end of bit or end of bit – 1TQ.

Comment C&S:

This behaviour is non-critically and will have no influence to the CAN Bus because the IUT drive dominant while the bus is already dominant.

6 Test List

Following test case numeration relates on the corresponding test specification.

Ref.	Description	Test script	Result	Comment
2	**Received frame type**			
2.1	*Valid frame format class*			
2.1.1	Identifier and number of data test in standard format DLC=0	10101001.TST	PASS	
2.1.1	Identifier and number of data test in standard format DLC=1	10101002.TST	PASS	
2.1.1	Identifier and number of data test in standard format DLC=2	10101003.TST	PASS	
2.1.1	Identifier and number of data test in standard format DLC=3	10101004.TST	PASS	
2.1.1	Identifier and number of data test in standard format DLC=4	10101005.TST	PASS	
2.1.1	Identifier and number of data test in standard format DLC=5	10101006.TST	PASS	
2.1.1	Identifier and number of data test in standard format DLC=6	10101007.TST	PASS	
2.1.1	Identifier and number of data test in standard format DLC=7	10101008.TST	PASS	
2.1.1	Identifier and number of data test in standard format DLC=8	10101009.TST	PASS	
2.1.2	Identifier and number of data in extended format-Test case 1 with DLC = 0	10102001.TST	PASS	
2.1.2	Identifier and number of data in extended format-Test case 1 with DLC = 1	10102002.TST	PASS	
2.1.2	Identifier and number of data in extended format-Test case 1 with DLC = 2	10102003.TST	PASS	
2.1.2	Identifier and number of data in extended format-Test case 1 with DLC = 3	10102004.TST	PASS	
2.1.2	Identifier and number of data in extended format-Test case 1 with DLC = 4	10102005.TST	PASS	
2.1.2	Identifier and number of data in extended format-Test case 1 with DLC = 5	10102006.TST	PASS	
2.1.2	Identifier and number of data in extended format-Test case 1 with DLC = 6	10102007.TST	PASS	
2.1.2	Identifier and number of data in extended format-Test case 1 with DLC = 7	10102008.TST	PASS	
2.1.2	Identifier and number of data in extended format-Test case 1 with DLC = 8	10102009.TST	PASS	
2.1.3	Identifier and number of data in extended format-Test case 2 with DLC = 0	10103001.TST	--	

Ref.	Description	Test script	Result	Comment
2.1.3	Identifier and number of data in extended format-Test case 2 with DLC = 1	10103002.TST	--	Not applicable. Designed for CAN version: B-passive
2.1.3	Identifier and number of data in extended format-Test case 2 with DLC = 2	10103003.TST	--	
2.1.3	Identifier and number of data in extended format-Test case 2 with DLC = 3	10103004.TST	--	
2.1.3	Identifier and number of data in extended format-Test case 2 with DLC = 4	10103005.TST	--	
2.1.3	Identifier and number of data in extended format-Test case 2 with DLC = 5	10103006.TST	--	
2.1.3	Identifier and number of data in extended format-Test case 2 with DLC = 6	10103007.TST	--	
2.1.3	Identifier and number of data in extended format-Test case 2 with DLC = 7	10103008.TST	--	
2.1.3	Identifier and number of data in extended format-Test case 2 with DLC = 8	10103009.TST	--	
2.1.4	Acceptance of non-nominal r1, r0 combination in standard format (r1=0 and r0=1)	10104001.TST	--	Not applicable. Designed for CAN version: A
2.1.4	Acceptance of non-nominal r1, r0 combination in standard format (r1=1 and r0=1)	10104002.TST	--	
2.1.4	Acceptance of non-nominal r1, r0 combination in standard format (r1=1 and r0=0)	10104003.TST	--	
2.1.5	Acceptance of « IDE,r0 » combination non-nominal value in standard format	10105000.TST	PASS	
2.1.6	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 1 (SRR=1; r1=1; r0=1)	10106001.TST	PASS	
2.1.6	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 1 (SRR=1; r1=1; r0=0)	10106002.TST	PASS	
2.1.6	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 1 (SRR=1; r1=0; r0=1)	10106003.TST	PASS	
2.1.6	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 1 (SRR=0; r1=1; r0=1)	10106004.TST	PASS	
2.1.6	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 1 (SRR=0; r1=1; r0=0)	10106005.TST	PASS	
2.1.6	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 1 (SRR=0; r1=0; r0=1)	10106006.TST	PASS	
2.1.6	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 1 (SRR=0; r1=0; r0=0)	10106007.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.1.7	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 2 (SRR=1; r1=1; r0=1)	10107001.TST	PASS	
2.1.7	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 2 (SRR=1; r1=1; r0=0)	10107002.TST	PASS	
2.1.7	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 2 (SRR=1; r1=0; r0=1)	10107003.TST	PASS	
2.1.7	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 2 (SRR=0; r1=1; r0=1)	10107004.TST	PASS	
2.1.7	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 2 (SRR=0; r1=1; r0=0)	10107005.TST	PASS	
2.1.7	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 2 (SRR=0; r1=0; r0=1)	10107006.TST	PASS	
2.1.7	Acceptance of non-nominal values of SRR, r1 and r0 in extended format-Test case 2 (SRR=0; r1=0; r0=0)	10107007.TST	PASS	
2.1.8	DLC greater than 8 (DLC = 9)	10108001.TST	PASS	
2.1.8	DLC greater than 8 (DLC = 10)	10108002.TST	PASS	
2.1.8	DLC greater than 8 (DLC = 11)	10108003.TST	PASS	
2.1.8	DLC greater than 8 (DLC = 12)	10108004.TST	PASS	
2.1.8	DLC greater than 8 (DLC = 13)	10108005.TST	PASS	
2.1.8	DLC greater than 8 (DLC = 14)	10108006.TST	PASS	
2.1.8	DLC greater than 8 (DLC = 15)	10108007.TST	PASS	
2.1.9	Absent bus idle (INTERM = 2)	10109001.TST	PASS	
2.1.9	Absent bus idle (INTERM = 3)	10109002.TST	PASS	
2.1.10	Stuff acceptance Test case 1 (IDEN=0x78; RTR=0; CTRL=0x08; Data=0x01E1E1E1E1E1E1E1)	10110001.TST	PASS	
2.1.10	Stuff acceptance-Test case 1 (IDEN=0x41F; RTR=0; CTRL=0x01; Data=0x00)	10110002.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.1.10	Stuff acceptance-Test case 1 (IDEN=0x707; RTR=0; CTRL=0x1F; Data=0x0F0F0F0F0F0F0F0F)	10110003.TST	PASS	
2.1.10	Stuff acceptance-Test case 1 (IDEN=0x360; RTR=0; CTRL=0x10; Data= -)	10110004.TST	PASS	
2.1.10	Stuff acceptance-Test case 1 (IDEN=0x730; RTR=0; CTRL=0x10; Data= -)	10110005.TST	PASS	
2.1.10	Stuff acceptance-Test case 1 (IDEN=0x47F; RTR=0; CTRL=0x01; Data= 0x1F)	10110006.TST	PASS	
2.1.10	Stuff acceptance-Test case 1 (IDEN=0x758; RTR=0; CTRL=0x00; Data= -)	10110007.TST	PASS	
2.1.10	Stuff acceptance-Test case 1 (IDEN=0x777; RTR=0; CTRL=0x01; Data=0x1F)	10110008.TST	PASS	
2.1.10	Stuff acceptance-Test case 1 (IDEN=0x7EF; RTR=1; CTRL=0x02; Data= -)	10110009.TST	PASS	
2.1.10	Stuff acceptance-Test case 1 (IDEN=0x3EA; RTR=1; CTRL=0x1F; Data= -)	10110010.TST	PASS	
2.1.11	Stuff acceptance-Test case 2 (IDEN1=0x1F0; IDEN2=0x30F0F; RTR=0; CTRL=0x08; Data=0x3C3C3C3C3C3C3C3C)	10111001.TST	PASS	
2.1.11	Stuff acceptance-Test case 2 (IDEN1=0x1F0; IDEN2=0x0F0F0; RTR=0; CTRL=0x01; Data=0x00)	10111002.TST	PASS	
2.1.11	Stuff acceptance-Test case 2 (IDEN1=0x078; IDEN2=0x00FF0; RTR=0; CTRL=0x1F; Data=0x0F0F0F0F0F0F0F0F)	10111003.TST	PASS	
2.1.11	Stuff acceptance-Test case 2 (IDEN1=0x078; IDEN2=0x00FF0; RTR=0; CTRL=0x3F; Data=0x1F0FE0F07FE0FF20)	10111004.TST	PASS	
2.1.11	Stuff acceptance-Test case 2 (IDEN1=0x7EE; IDEN2=0x00000; RTR=0; CTRL=0x01; Data=0xA0)	10111005.TST	PASS	
2.1.11	Stuff acceptance-Test case 2 (IDEN1=0x02F; IDEN2=0x0540F; RTR=1; CTRL=0x20; Data=-)	10111006.TST	PASS	
2.1.11	Stuff acceptance-Test case 2 (IDEN1=0x557; IDEN2=0x15557; RTR=1; CTRL=0x3F; Data=-)	10111007.TST	PASS	
2.1.12	Message validation (7th bit of EOF inverted)	10112000.TST	PASS	
~~2.1.13~~	~~DLC not belonging to NDATA~~	--	--	Not applicable with CAN version {A,B-passive, B}
2.1.14	Receive part of 3.1.3 Arbitration in standard format frame ID=_11 1110 1111	10114001.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.1.14	Receive part of 3.1.3 Arbitration in standard format frame ID=1_1 1110 1111	10114002.TST	PASS	
2.1.14	Receive part of 3.1.3 Arbitration in standard format frame ID=111 _110 1111	10114003.TST	PASS	
2.1.14	Receive part of 3.1.3 Arbitration in standard format frame ID=11_ 1110 1111	10114004.TST	PASS	
2.1.14	Receive part of 3.1.3 Arbitration in standard format frame ID=111 1_10 1111	10114005.TST	PASS	
2.1.14	Receive part of 3.1.3 Arbitration in standard format frame ID=111 11_0 1111	10114006.TST	PASS	
2.1.14	Receive part of 3.1.3 Arbitration in standard format frame ID=111 1110 _111	10114007.TST	PASS	
2.1.14	Receive part of 3.1.3 Arbitration in standard format frame ID=111 1110 1_11	10114008.TST	PASS	
2.1.14	Receive part of 3.1.3 Arbitration in standard format frame ID=111 1110 11_1	10114009.TST	PASS	
2.1.14	Receive part of 3.1.3 Arbitration in standard format frame ID=111 1110 111_	10114010.TST	PASS	
2.1.14	Receive part of 3.1.3 Arbitration in RTR standard format frame Test 1	10114011.TST	PASS	
2.1.14	Receive part of 3.1.3 Arbitration in RTR standard format frame Test 2	10114012.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 1	10115001.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 2	10115002.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 3	10115003.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 4	10115004.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 5	10115005.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 6	10115006.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 7	10115007.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 8	10115008.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 9	10115009.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 10	10115010.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 11	10115011.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 12	10115012.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 13	10115013.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 14	10115014.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 15	10115015.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 16	10115016.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 17	10115017.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 18	10115018.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 19	10115019.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 20	10115020.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 21	10115021.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 22	10115022.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 23	10115023.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 24	10115024.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 25	10115025.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 26	10115026.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 27	10115027.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 28	10115028.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 29	10115029.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 30	10115030.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 31	10115031.TST	PASS	
2.1.15	Receive part of 3.1.4 Arbitration in extended format frame Test 32	10115032.TST	PASS	
2.2	*Error detection class*			
2.2.1	Bit error in data frame (ACK forced to recessive)	10201000.TST	PASS	
2.2.2	Stuff error-Test case 1 (SOF, 0x078 [5, INV]...)	10202001.TST	PASS	
2.2.2	Stuff error-Test case 1 (SOF, 0x078 [10, INV]...)	10202002.TST	PASS	
2.2.2	Stuff error-Test case 1 (0x078, RTR_0 [2, INV]...)	10202003.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [3, INV]...)	10202004.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [9, INV]...)	10202005.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [14, INV]...)	10202006.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [19, INV]...)	10202007.TST	PASS	
2.2.2	Stuff error-Test case 1 (0x01E1E1E1E1E1E1E1 [24, INV]...)	10202008.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [29, INV]...)	10202009.TST	PASS	
2.2.2	Stuff error-Test case 1 Data (DLC_8, 0x01E1E1E1E1E1E1E1 [34, INV]...)	10202010.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [39, INV]...)	10202011.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [44, INV]...)	10202012.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [49, INV]...)	10202013.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [54, INV]...)	10202014.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [59, INV]...)	10202015.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [64, INV]...)	10202016.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [69, INV]...)	10202017.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [74, INV]...)	10202018.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_8, 0x01E1E1E1E1E1E1E1 [79, INV]...)	10202019.TST	PASS	
2.2.2	Stuff error-Test case 1 (SOF, 0x41F [7, INV]...)	10202020.TST	PASS	
2.2.2	Stuff error-Test case 1 (SOF, 0x41F [12, INV]...)	10202021.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_1 [3, INV]...)	10202022.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_1, 0x00 [6, INV]...)	10202023.TST	PASS	
2.2.2	Stuff error-Test case 1 (CRC [3, INV]...)	10202024.TST	PASS	
2.2.2	Stuff error-Test case 1 (SOF, 0x707 [9, INV]...)	10202025.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15 [5, INV]...)	10202026.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [5, INV]...)	10202027.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [10, INV]...)	10202028.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [15, INV]...)	10202029.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [20, INV]...)	10202030.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [25, INV]…)	10202031.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [30, INV]…)	10202032.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [35, INV]...)	10202033.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [40, INV]...)	10202034.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [45, INV]...)	10202035.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [50, INV]...)	10202036.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [55, INV]...)	10202037.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [60, INV]...)	10202038.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [65, INV]...)	10202039.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [70, INV]...)	10202040.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [75, INV]...)	10202041.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15, 0x0F0F0F0F0F0F0F0F [80, INV]...)	10202042.TST	PASS	
2.2.2	Stuff error-Test case 1 (SOF, 0x360 [12, INV]...)	10202043.TST	PASS	
2.2.2	Stuff error-Test case 1 (CRC [2, INV]...)	10202044.TST	PASS	
2.2.2	Stuff error-Test case 1 (CRC [18, INV]...)	10202045.TST	PASS	
2.2.2	Stuff error-Test case 1 (CRC [7, INV]...)	10202046.TST	PASS	
2.2.2	Stuff error-Test case 1 (RTR_0 [2, INV]...)	10202047.TST	PASS	
2.2.2	Stuff error-Test case 1 (CRC [2, INV]...)	10202048.TST	PASS	
2.2.2	Stuff error-Test case 1 (CRC [10, INV]...)	10202049.TST	PASS	
2.2.2	Stuff error-Test case 1 (CRC [18, INV]...)	10202050.TST	PASS	
2.2.2	Stuff error-Test case 1 (SOF, 0x47F [10, INV]...)	10202051.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.2.2	Stuff error-Test case 1 (DLC_1 [3, INV]...)	10202052.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_1, 0x1F [9, INV]...)	10202053.TST	PASS	
2.2.2	Stuff error-Test case 1 (IDE_0 [2, INV]...)	10202054.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_0 [5, INV]...)	10202055.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_1 [3, INV]...)	10202056.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_1, 0x1F [9, INV]...)	10202057.TST	PASS	
2.2.2	Stuff error-Test case 1 (SOF, 0x7EF [6, INV]...)	10202058.TST	PASS	
2.2.2	Stuff error-Test case 1 (RTR_1 [2, INV]...)	10202059.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_2 [3, INV]...)	10202060.TST	PASS	
2.2.2	Stuff error-Test case 1 (CRC [15, INV]...)	10202061.TST	PASS	
2.2.2	Stuff error-Test case 1 (SOF, 0x3EA [7, INV]...)	10202062.TST	PASS	
2.2.2	Stuff error-Test case 1 (DLC_15 [5, INV]...)	10202063.TST	PASS	
2.2.3	Stuff error-Test case 2 (SOF, 0x1F0 [8, INV]...)	10203001.TST	PASS	
2.2.3	Stuff error-Test case 2 (SOF, 0x1F0 [13, INV]...)	10203002.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x30F0F [3, INV]...)	10203003.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x30F0F [8, INV]...)	10203004.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x30F0F [13, INV]...)	10203005.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x30F0F [18, INV]...)	10203006.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x30F0F [23, INV]...)	10203007.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C [3, INV]...)	10203008.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C [8, INV]...)	10203009.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C [13, INV]...)	10203010.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C [18, INV]...)	10203011.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C [23, INV]...)	10203012.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C [28, INV]...)	10203013.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C3C [33, INV]...)	10203014.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C3C [38, INV]...)	10203015.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C3C [43, INV]...)	10203016.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C3C [48, INV]...)	10203017.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C3C [53, INV]...)	10203018.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C3C [58, INV]...)	10203019.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C3C [63, INV]...)	10203020.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C3C [68, INV]...)	10203021.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C3C [73, INV]...)	10203022.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_8, 0x3C3C3C3C3C3C3C3C3C [78, INV]...)	10203023.TST	PASS	
2.2.3	Stuff error-Test case 2 (ID=0x00000000; CRC[13, INV]...)	10203024.TST	PASS	
2.2.3	Stuff error-Test case 2 (SOF, 0x1F0 [8, INV]...)	10203025.TST	PASS	
2.2.3	Stuff error-Test case 2 (SOF, 0x1F0 [13, INV]...)	10203026.TST	PASS	
2.2.3	Stuff error-Test case 2 (RTR_0 [2, INV]...)	10203027.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_1 [4, INV]...)	10203028.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_1, 0x00 [6, INV]...)	10203029.TST	PASS	
2.2.3	Stuff error-Test case 2 (SOF, 0x078 [5, INV]...)	10203030.TST	PASS	
2.2.3	Stuff error-Test case 2 (SOF, 0x078 [10, INV]...)	10203031.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15 [5, INV]...)	10203032.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [5, INV]...)	10203033.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [10, INV]...)	10203034.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [15, INV]...)	10203035.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [20, INV]...)	10203036.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [25, INV]...)	10203037.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [30, INV]...)	10203038.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [35, INV]...)	10203039.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [40, INV]...)	10203040.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [45, INV]...)	10203041.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [50, INV]...)	10203042.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [55, INV]...)	10203043.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [60, INV]...)	10203044.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [65, INV]...)	10203045.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [70, INV]...)	10203046.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [75, INV]...)	10203047.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F [80, INV]...)	10203048.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15, 0x0F0F0F0F0F0F0F0F, CRC [11, INV]...)	10203049.TST	PASS	
2.2.3	Stuff error-Test case 2 (SOF, 0x078 [5, INV...)	10203050.TST	PASS	
2.2.3	Stuff error-Test case 2 (SOF, 0x078 [10, INV]...)	10203051.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x00FF0 [6, INV]...)	10203052.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x00FF0 [13, INV]...)	10203053.TST	PASS	
2.2.3	Stuff error-Test case 2 (RTR_0 [2, INV]...)	10203054.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12 [3, INV]...)	10203055.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [3, INV]...)	10203056.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [10, INV]...)	10203057.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [15, INV]...)	10203058.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [20, INV]...)	10203059.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [29, INV]...)	10203060.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [34, INV]...)	10203061.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [39, INV]...)	10203062.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [46, INV]...)	10203063.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [52, INV]...)	10203064.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [57, INV]...)	10203065.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [64, INV]...)	10203066.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_12, 0x1F0FE0F07FE0FF20 [76, INV]...)	10203067.TST	PASS	
2.2.3	Stuff error-Test case 2 (CRC [11, INV]...)	10203068.TST	PASS	
2.2.3	Stuff error-Test case 2 (SOF, 0x7EE [6, INV]...)	10203069.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x000 [6, INV]...)	10203070.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x000 [12, INV]...)	10203071.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x000 [18, INV]...)	10203072.TST	PASS	
2.2.3	Stuff error-Test case 2 (r1_0 [2, INV]...)	10203073.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_1, 0xA0 [9, INV]...)	10203074.TST	PASS	
2.2.3	Stuff error-Test case 2 (SOF, 0x02F [5, INV]...)	10203075.TST	PASS	
2.2.3	Stuff error-Test case 2 (SRR_1 [2, INV]...)	10203076.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1, 0x0540F [14, INV]...)	10203077.TST	PASS	
2.2.3	Stuff error-Test case 2 (RTR_1 [2, INV]...)	10203078.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_0 [5, INV]...)	10203079.TST	PASS	
2.2.3	Stuff error-Test case 2 (CRC [16, INV]...)	10203080.TST	PASS	
2.2.3	Stuff error-Test case 2 (IDE_1 [2, INV]...)	10203081.TST	PASS	
2.2.3	Stuff error-Test case 2 (r1_1 [2, INV]...)	10203082.TST	PASS	
2.2.3	Stuff error-Test case 2 (DLC_15 [5, INV]...)	10203083.TST	PASS	
2.2.4	CRC error - Dominant bit inverted	10204001.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.2.4	CRC error - Recessive bit inverted	10204002.TST	PASS	
2.2.5	Combination of CRC error and FORM error test	10205000.TST	PASS	
2.2.6	Form error in data frame - Test case 1	10206000.TST	PASS	
2.2.7	Form error in data frame - Test case 2	10207000.TST	PASS	
2.2.8	Form error in data frame - Test case 3 (EOF [1, INV])	10208001.TST	PASS	
2.2.8	Form error in data frame - Test case 3 (EOF [3, INV])	10208002.TST	PASS	
2.2.8	Form error in data frame - Test case 3 (EOF [6, INV])	10208003.TST	PASS	
2.2.9	Message non-validation	10209000.TST	PASS	
2.3	*Error Frame management class*			
2.3.1	Error flag longer than 6 bits (1 bit longer)	10301001.TST	PASS	
2.3.1	Error flag longer than 6 bits (4 bits longer)	10301002.TST	PASS	
2.3.1	Error flag longer than 6 bits (7 bits longer)	10301003.TST	PASS	
2.3.2	Data frame starting on third bit of the intermission field	10302000.TST	PASS	
2.3.3	Bit error in error flag (1st bit)	10303001.TST	PASS	
2.3.3	Bit error in error flag (3rd bit)	10303002.TST	PASS	
2.3.3	Bit error in error flag (6th bit)	10303003.TST	PASS	
2.3.4	Form error in error delimiter (2nd bit)	10304001.TST	PASS	
2.3.4	Form error in error delimiter (4th bit)	10304002.TST	PASS	
2.3.4	Form error in error delimiter (7th bit)	10304003.TST	PASS	
2.4	*Overload Frame management class*			
2.4.1	MAC overload generation during intermission field (1st bit inverted)	10401001.TST	PASS	
2.4.1	MAC overload generation during intermission field (2nd bit inverted)	10401002.TST	PASS	
2.4.2	Last bit of EOF	10402000.TST	PASS	
2.4.3	Eighth bit of an error and overload delimiter (Error frame)	10403001.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.4.3	Eighth bit of an error and overload delimiter (Overload frame)	10403002.TST	PASS	
2.4.4	Bit error in overload flag (1st bit)	10404001.TST	PASS	
2.4.4	Bit error in overload flag (3rd bit)	10404002.TST	PASS	
2.4.4	Bit error in overload flag (6th bit)	10404003.TST	PASS	
2.4.5	Form error in overload delimiter (2nd bit)	10405001.TST	PASS	
2.4.5	Form error in overload delimiter (4th bit)	10405002.TST	PASS	
2.4.5	Form error in overload delimiter (7th bit)	10405003.TST	PASS	
2.4.6	MAC overload generation during intermission field following an error frame (1st bit)	10406001_CS.TST	PASS	C&S Add-on Test
2.4.6	MAC overload generation during intermission field following an error frame (2nd bit)	10406002_CS.TST	PASS	C&S Add-on Test
2.4.7	MAC overload generation during intermission field following an overl. frame (1st bit)	10407001_CS.TST	PASS	C&S Add-on Test
2.4.7	MAC overload generation during intermission field following an overl. frame (2nd bit)	10407002_CS.TST	PASS	C&S Add-on Test
2.5	*Passive error state class*			
2.5.1	Passive-error flag completion-Test case 1 (1st bit)	10501001.TST	PASS	
2.5.1	Passive-error flag completion-Test case 1 (3rd bit)	10501002.TST	PASS	
2.5.1	Passive-error flag completion-Test case 1 (6th bit)	10501003.TST	PASS	
2.5.2	Data frame acceptance after passive-error frame transmission	10502000.TST	PASS	
2.5.3	Acceptance of 7 consecutive dominant bits after passive-error flag (1st bit)	10503001.TST	PASS	
2.5.3	Acceptance of 7 consecutive dominant bits after passive-error flag (4th bit)	10503002.TST	PASS	
2.5.3	Acceptance of 7 consecutive dominant bits after passive-error flag (7th bit)	10503003.TST	PASS	
2.5.4	Passive state unchanged on further errors	10504000.TST	PASS	
2.5.5	Passive-error flag completion-Test case 2 (1st bit)	10505001.TST	PASS	
2.5.5	Passive-error flag completion-Test case 2 (3rd bit)	10505002.TST	PASS	
2.5.5	Passive-error flag completion-Test case 2 (6th bit)	10505003.TST	PASS	
2.5.6	Form error in passive-error delimiter (2nd bit)	10506001.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.5.6	Form error in passive-error delimiter (4th bit)	10506002.TST	PASS	
2.5.6	Form error in passive-error delimiter (7th bit)	10506003.TST	PASS	
2.5.7	Transition from Active to Passive ERROR FLAG	10507000_CS.TST	PASS	C&S Add-on Test
2.6	*Error counter management class*			
2.6.1	REC increment on bit error in active-error flag (1st bit)	10601001.TST	PASS	
2.6.1	REC increment on bit error in active-error flag (3rd bit)	10601002.TST	PASS	
2.6.1	REC increment on bit error in active-error flag (6th bit)	10601003.TST	PASS	
2.6.2	REC increment on bit error in overload flag (1st bit)	10602001.TST	PASS	
2.6.2	REC increment on bit error in overload flag (4th bit)	10602002.TST	PASS	
2.6.2	REC increment on bit error in overload flag (6th bit)	10602003.TST	PASS	
2.6.3	REC increment when active-error flag is longer than 13 bits	10603000.TST	PASS	
2.6.4	REC increment when overload flag is longer than 13 bits	10604000.TST	PASS	
2.6.5	REC increment on bit error in the ACK field	10605000.TST	PASS	
2.6.6	REC increment on form error in CRC delimiter	10606000.TST	PASS	
2.6.7	REC increment on form error in ACK delimiter	10607000.TST	PASS	
2.6.8	REC increment on form error in EOF field (2nd bit)	10608001.TST	PASS	
2.6.8	REC increment on form error in EOF field (3rd bit)	10608002.TST	PASS	
2.6.8	REC increment on form error in EOF field (5th bit)	10608003.TST	PASS	
2.6.9	REC increment on stuff error (IDEN field - 5th bit)	10609001.TST	PASS	
2.6.9	REC increment on stuff error (IDEN field - 10th bit)	10609002.TST	PASS	
2.6.9	REC increment on stuff error	10609003.TST	PASS	
2.6.9	REC increment on stuff error	10609004.TST	PASS	
2.6.9	REC increment on stuff error (DATA field - 14th bit)	10609005.TST	PASS	
2.6.9	REC increment on stuff error (DATA field - 24th bit)	10609006.TST	PASS	

Ref.	Description	Test script	Result	Comment
2.6.9	REC increment on stuff error (CRC field - 2nd bit)	10609007.TST	PASS	
2.6.9	REC increment on stuff error (CRC field - 8th bit)	10609008.TST	PASS	
2.6.10	REC increment on CRC error	10610000.TST	PASS	
2.6.11	REC increment on dominant bit after the end of an error flag	10611000.TST	PASS	
2.6.12	REC increment on form error in error delimiter (2nd bit)	10612001.TST	PASS	
2.6.12	REC increment on form error in error delimiter (7th bit)	10612002.TST	PASS	
2.6.13	REC increment on form error in overload delimiter (2nd bit)	10613001.TST	PASS	
2.6.13	REC increment on form error in overload delimiter (7th bit)	10613002.TST	PASS	
2.6.14	REC decrement on valid frame reception	10614000.TST	PASS	
2.6.15	REC decrement on valid frame reception during passive state	10615000.TST	PASS	
2.6.16	REC non-increment on last bit of EOF field	10616000.TST	PASS	
2.6.17	REC non-increment on 13-bit length overload flag	10617000.TST	PASS	
2.6.18	REC non-increment on 13-bit length error flag	10618000.TST	PASS	
2.6.19	REC non-increment on last bit of error and overload delimiter (Error Test)	10619001.TST	PASS	
2.6.19	REC non-increment on last bit of error and overload delimiter (Overload Test)	10619002_CS.TST	PASS	C&S Add-on Test
2.6.20	REC non-decrement on transmission	10620000_CS.TST	PASS	C&S Add-on Test
2.6.21	REC non-decrement on transmission and no REC increment on transmission-error	10620001_CS.TST	PASS	C&S Add-on Test
2.7	*Bit timing class*			See: Generation of bit timing atoms
3	**Transmitted frame type**			
3.1	*Valid frame format class*			
3.1.1	Identifier and number of data bytes in standard format (DLC=0)	20101001.TST	PASS	
3.1.1	Identifier and number of data bytes in standard format (DLC=1)	20101002.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.1.1	Identifier and number of data bytes in standard format (DLC=2)	20101003.TST	PASS	
3.1.1	Identifier and number of data bytes in standard format (DLC=3)	20101004.TST	PASS	
3.1.1	Identifier and number of data bytes in standard format (DLC=4)	20101005.TST	PASS	
3.1.1	Identifier and number of data bytes in standard format (DLC=5)	20101006.TST	PASS	
3.1.1	Identifier and number of data bytes in standard format (DLC=6)	20101007.TST	PASS	
3.1.1	Identifier and number of data bytes in standard format (DLC=7)	20101008.TST	PASS	
3.1.1	Identifier and number of data bytes in standard format (DLC=8)	20101009.TST	PASS	
3.1.2	Identifier and number of data bytes in extended format (DLC=0)	20102001.TST	PASS	
3.1.2	Identifier and number of data bytes in extended format (DLC=1)	20102002.TST	PASS	
3.1.2	Identifier and number of data bytes in extended format (DLC=2)	20102003.TST	PASS	
3.1.2	Identifier and number of data bytes in extended format (DLC=3)	20102004.TST	PASS	
3.1.2	Identifier and number of data bytes in extended format (DLC=4)	20102005.TST	PASS	
3.1.2	Identifier and number of data bytes in extended format (DLC=5)	20102006.TST	PASS	
3.1.2	Identifier and number of data bytes in extended format (DLC=6)	20102007.TST	PASS	
3.1.2	Identifier and number of data bytes in extended format (DLC=7)	20102008.TST	PASS	
3.1.2	Identifier and number of data bytes in extended format (DLC=8)	20102009.TST	PASS	
3.1.3	Arbitration in standard format frame ID=_11 1110 1111	20103001.TST	PASS	
3.1.3	Arbitration in standard format frame ID=1_1 1110 1111	20103002.TST	PASS	
3.1.3	Arbitration in standard format frame ID=11_ 1110 1111	20103003.TST	PASS	
3.1.3	Arbitration in standard format frame ID=111 _110 1111	20103004.TST	PASS	
3.1.3	Arbitration in standard format frame ID=111 1_10 1111	20103005.TST	PASS	
3.1.3	Arbitration in standard format frame ID=111 11_0 1111	20103006.TST	PASS	
3.1.3	Arbitration in standard format frame ID=111 1110 _111	20103007.TST	PASS	
3.1.3	Arbitration in standard format frame ID=111 1110 1_11	20103008.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.1.3	Arbitration in standard format frame ID=111 1110 11_1	20103009.TST	PASS	
3.1.3	Arbitration in standard format frame ID=111 1110 111_	20103010.TST	PASS	
3.1.3	Arbitration in RTR standard format frame Test 1	20103011.TST	PASS	
3.1.3	Arbitration in RTR standard format frame Test 2	20103012.TST	PASS	
3.1.4	Arbitration in extended format frame Test 1	20104001.TST	PASS	
3.1.4	Arbitration in extended format frame Test 2	20104002.TST	PASS	
3.1.4	Arbitration in extended format frame Test 3	20104003.TST	PASS	
3.1.4	Arbitration in extended format frame Test 4	20104004.TST	PASS	
3.1.4	Arbitration in extended format frame Test 5	20104005.TST	PASS	
3.1.4	Arbitration in extended format frame Test 6	20104006.TST	PASS	
3.1.4	Arbitration in extended format frame Test 7	20104007.TST	PASS	
3.1.4	Arbitration in extended format frame Test 8	20104008.TST	PASS	
3.1.4	Arbitration in extended format frame Test 9	20104009.TST	PASS	
3.1.4	Arbitration in extended format frame Test 10	20104010.TST	PASS	
3.1.4	Arbitration in extended format frame Test 11	20104011.TST	PASS	
3.1.4	Arbitration in extended format frame Test 12	20104012.TST	PASS	
3.1.4	Arbitration in extended format frame Test 13	20104013.TST	PASS	
3.1.4	Arbitration in extended format frame Test 14	20104014.TST	PASS	
3.1.4	Arbitration in extended format frame Test 15	20104015.TST	PASS	
3.1.4	Arbitration in extended format frame Test 16	20104016.TST	PASS	
3.1.4	Arbitration in extended format frame Test 17	20104017.TST	PASS	
3.1.4	Arbitration in extended format frame Test 18	20104018.TST	PASS	
3.1.4	Arbitration in extended format frame Test 19	20104019.TST	PASS	
3.1.4	Arbitration in extended format frame Test 20	20104020.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.1.4	Arbitration in extended format frame Test 21	20104021.TST	PASS	
3.1.4	Arbitration in extended format frame Test 22	20104022.TST	PASS	
3.1.4	Arbitration in extended format frame Test 23	20104023.TST	PASS	
3.1.4	Arbitration in extended format frame Test 24	20104024.TST	PASS	
3.1.4	Arbitration in extended format frame Test 25	20104025.TST	PASS	
3.1.4	Arbitration in extended format frame Test 26	20104026.TST	PASS	
3.1.4	Arbitration in extended format frame Test 27	20104027.TST	PASS	
3.1.4	Arbitration in extended format frame Test 28	20104028.TST	PASS	
3.1.4	Arbitration in extended format frame Test 29	20104029.TST	PASS	
3.1.4	Arbitration in extended format frame Test 30	20104030.TST	PASS	
3.1.4	Arbitration in extended format frame Test 31	20104031.TST	PASS	
3.1.4	Arbitration in extended format frame Test 32	20104032.TST	PASS	
3.1.5	Message validation	20105000.TST	PASS	
3.1.6	Stuff bit generation capability in standard frame - Frame 1	20106001.TST	PASS	
3.1.6	Stuff bit generation capability in standard frame - Frame 2	20106002.TST	PASS	
3.1.6	Stuff bit generation capability in standard frame - Frame 3	20106003.TST	PASS	
3.1.6	Stuff bit generation capability in standard frame - Frame 4	20106004.TST	PASS	
3.1.6	Stuff bit generation capability in standard frame - Frame 5	20106005.TST	PASS	
3.1.6	Stuff bit generation capability in standard frame - Frame 6	20106006.TST	PASS	
3.1.7	Stuff bit generation capability in extended frame - Frame 1	20107001.TST	PASS	
3.1.7	Stuff bit generation capability in extended frame - Frame 2	20107002.TST	PASS	
3.1.7	Stuff bit generation capability in extended frame - Frame 3	20107003.TST	PASS	
3.2	*Error detection class*			
3.2.1	Bit error in standard frame test (SOF)	20201001.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.2.1	Bit error in standard frame test (ID)	20201002.TST	PASS	
3.2.1	Bit error in standard frame test (DLC bit 3)	20201003.TST	PASS	
3.2.1	Bit error in standard frame test (DLC bit 4)	20201004.TST	PASS	
3.2.1	Bit error in standard frame test (Data bit 1)	20201005.TST	PASS	
3.2.1	Bit error in standard frame test (Data bit 1)	20201006.TST	PASS	
3.2.1	Bit error in standard frame test (CRC bit 13)	20201007.TST	PASS	
3.2.1	Bit error in standard frame test (CRC bit 8)	20201008.TST	PASS	
3.2.1	Bit error in standard frame test (RTR)	20201009.TST	PASS	
3.2.1	Bit error in standard frame test (r0)	20201010.TST	PASS	
3.2.1	Bit error in standard frame test (CRC_DEL)	20201011.TST	PASS	
3.2.1	Bit error in standard frame test (ACK_DEL)	20201012.TST	PASS	
3.2.1	Bit error in standard frame test (IDE_0)	20201013.TST	PASS	
3.2.2	Bit error in extended frame test (SOF)	20202001.TST	PASS	
3.2.2	Bit error in extended frame test (ID)	20202002.TST	PASS	
3.2.2	Bit error in extended frame test (DLC bit 5)	20202003.TST	PASS	
3.2.2	Bit error in extended frame test (DLC bit 4)	20202004.TST	PASS	
3.2.2	Bit error in extended frame test (Data bit 2)	20202005.TST	PASS	
3.2.2	Bit error in extended frame test (Data bit 1)	20202006.TST	PASS	
3.2.2	Bit error in extended frame test (CRC bit 10)	20202007.TST	PASS	
3.2.2	Bit error in extended frame test (CRC bit 12)	20202008.TST	PASS	
3.2.2	Bit error in extended frame test (RTR)	20202009.TST	PASS	
3.2.2	Bit error in extended frame test (r0)	20202010.TST	PASS	
3.2.2	Bit error in extended frame test (r1)	20202011.TST	PASS	
3.2.2	Bit error in extended frame test (CRC_DEL)	20202012.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.2.2	Bit error in extended frame test (ACK_DEL)	20202013.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203001.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203002.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203003.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203004.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203005.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203006.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203007.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203008.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203009.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203010.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203011.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203012.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203013.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203014.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203015.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203016.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203017.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203018.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 1)	20203019.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 2)	20203020.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 2)	20203021.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 2)	20203022.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 2)	20203023.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.2.3	Stuff error test in standard frame (Test Frame 2)	20203024.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 3)	20203025.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 3)	20203026.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 3)	20203027.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 4)	20203028.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 4)	20203029.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 5)	20203030.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 5)	20203031.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 6)	20203032.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 6)	20203033.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 6)	20203034.TST	PASS	
3.2.3	Stuff error test in standard frame (Test Frame 6)	20203035.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204001.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204002.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204003.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204004.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204005.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204006.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204007.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204008.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204009.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204010.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204011.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204012.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204013.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204014.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204015.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204016.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204017.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204018.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204019.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204020.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204021.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204022.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 1)	20204023.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 2)	20204024.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 2)	20204025.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 2)	20204026.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 2)	20204027.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 2)	20204028.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 3)	20204029.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 3)	20204030.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 3)	20204031.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 3)	20204032.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 3)	20204033.TST	PASS	
3.2.4	Stuff error test in extended frame (Test Frame 3)	20204034.TST	PASS	
3.2.4	Stuff error test in extended frame (C&S Add-on)	20204035.TST	PASS	
3.2.5	Form error (CRC Delimiter)	20205001.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.2.5	Form error (ACK Delimiter)	20205002.TST	PASS	
3.2.5	Form error (EOF bit 1)	20205003.TST	PASS	
3.2.5	Form error (EOF bit 4)	20205004.TST	PASS	
3.2.5	Form error (EOF bit 7)	20205005.TST	PASS	
3.2.6	Acknowledgement error	20206000.TST	PASS	
3.3	*Error frame management class*			
3.3.1	Error flag longer than 6 bits (1 bit longer)	20301001.TST	PASS	
3.3.1	Error flag longer than 6 bits (4 bits longer)	20301002.TST	PASS	
3.3.1	Error flag longer than 6 bits (7 bits longer)	20301003.TST	PASS	
3.3.2	Transmission on the third bit of intermission field	20302000.TST	PASS	
3.3.2	Transmission on the third bit of intermission field with recessive ID bits - Test 2 (C&S Add-on)	20302001_CS.TST	PASS	C&S Add-on Test
3.3.2	Transmission on the third bit of intermission field with recessive ID bits - Test 3 (C&S Add-on)	20302002_CS.TST	PASS	C&S Add-on Test
3.3.2	Transmission on the third bit of intermission field - Test 4 (C&S Add-on)	20302003_CS.TST	PASS	C&S Add-on Test
3.3.2	Transmission on the third bit of intermission field - Test 5 (C&S Add-on)	20302004_CS.TST	PASS	C&S Add-on Test
3.3.2	Transmission on the third bit of intermission field - Test 6 (C&S Add-on)	20302005_CS.TST	PASS	C&S Add-on Test
3.3.2	Transmission on the third bit of intermission field - Test 7 (C&S Add-on)	20302006_CS.TST	PASS	C&S Add-on Test
3.3.3	Bit error in error flag (1st Bit)	20303001.TST	PASS	
3.3.3	Bit error in error flag (4th bit)	20303002.TST	PASS	
3.3.3	Bit error in error flag (7th bit)	20303003.TST	PASS	
3.3.4	Form error in error delimiter (1st bit - C&S Add-on)	20304001_CS.TST	PASS	C&S Add-on Test
3.3.4	Form error in error delimiter (2nd bit)	20304002.TST	PASS	
3.3.4	Form error in error delimiter (3rd bit - C&S Add-on)	20304003_CS.TST	PASS	C&S Add-on Test
3.3.4	Form error in error delimiter (4th bit)	20304004.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.3.4	Form error in error delimiter (5th bit - C&S Add-on)	20304005_CS.TST	PASS	C&S Add-on Test
3.3.4	Form error in error delimiter (6th bit - C&S Add-on)	20304006_CS.TST	PASS	C&S Add-on Test
3.3.4	Form error in error delimiter (7th bit)	20304007.TST	PASS	
3.3.4	Form error in error delimiter (8th bit - C&S Add-on)	20304008_CS.TST	PASS	C&S Add-on Test
3.4	*Overload frame management class*			
3.4.1	MAC overload generation in intermission field (1st bit)	20401001.TST	PASS	
3.4.1	MAC overload generation in intermission field (2nd bit)	20401002.TST	PASS	
3.4.2	Eight bit of an error delimiter	20402001.TST	PASS	
3.4.2	Eight bit of an overload delimiter	20402002.TST	PASS	
3.4.3	Transmission on the third bit of intermission field (ID=0x111)	20403000.TST	PASS	
3.4.3	Transmission on the third bit of intermission field with recessive ID bits (ID=0x7EF - C&S Add-on)	20403001_cs.tst	PASS	C&S Add-on Test
3.4.4	Bit error in overload flag (1st bit)	20404001.TST	PASS	
3.4.4	Bit error in overload flag (2nd bit)	20404002.TST	PASS	
3.4.4	Bit error in overload flag (6th bit)	20404003.TST	PASS	
3.4.5	Form error in overload delimiter (2nd bit)	20405001.TST	PASS	
3.4.5	Form error in overload delimiter (4th bit)	20405002.TST	PASS	
3.4.5	Form error in overload delimiter (7th bit)	20405003.TST	PASS	
3.5	*Passive error state and bus-off class*			
3.5.1	Acceptance of active-error flag overwriting passive-error flag (1st bit)	20501001.TST	PASS	
3.5.1	Acceptance of active-error flag overwriting passive-error flag (3rd bit)	20501002.TST	PASS	
3.5.1	Acceptance of active-error flag overwriting passive-error flag (6th bit)	20501003.TST	PASS	
3.5.2	Frame acceptance after passive-error frame transmission	20502000.TST	PASS	
3.5.3	Acceptance of 7 consecutive dominant bits after Passive-error flag (1 bit forced dominant)	20503001.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.5.3	Acceptance of 7 consecutive dominant bits after Passive-error flag (2 bits forced dominant)	20503002.TST	PASS	
3.5.3	Acceptance of 7 consecutive dominant bits after Passive-error flag (3 bits forced dominant)	20503003.TST	PASS	
3.5.4	Reception of frame during suspend transmission field (Suspend=0)	20504001.TST	PASS	
3.5.4	Reception of frame during suspend transmission field (Suspend=3)	20504002.TST	PASS	
3.5.4	Reception of frame during suspend transmission field (Suspend=7)	20504003.TST	PASS	
3.5.5	Transmission of frame after suspend transmission field - Test case 1	20505000.TST	PASS	
3.5.6	Transmission of frame after suspend transmission field - Test case 2	20506000.TST	PASS	
3.5.7	Transmission of frame after suspend transmission field - Test case 3	20507000.TST	PASS	
3.5.8	Transmission of frame without suspend transmission field (TEC Passive, after reception)	20508000.TST	PASS	
3.5.8	Transmission of frame after the 2nd bit of Intermission field (TEC Passive, after receive state)	20508001_CS.TST	EXEC	C&S Add-on Test execute only
3.5.8	Transmission of frame after the 2nd bit of Intermission field (REC Passive, after receive state)	20508002_CS.TST	EXEC	
3.5.8	Transmission of frame after the 2nd bit of Intermission field (REC Passive, after reception)	20508003_CS.TST	EXEC	
3.5.8	Transmission of frame without suspend transmission field (REC Passive, after reception)	20508004_CS.TST	PASS	C&S Add-on Test
3.5.9	No-transmission of frame on the third bit of intermission field	20509000.TST	PASS	
3.5.9	No-transmission of frame on the 7th bit of suspend field	20509001_CS.TST	PASS	C&S Add-on Test
3.5.9	No-transmission of frame on the 1st bit of suspend field	20509002_CS.TST	PASS	C&S Add-on Test
3.5.9	No transmission of frame after the 3rd bit of Intermission field (without Suspend)	20509003_CS.TST	PASS	C&S Add-on Test
3.5.10	Bus-off state	20510000.TST	PASS	
3.5.10	Bus-off state (C&S Add-on)	20510001_CS.TST	PASS	C&S Add-on Test
3.5.11	Bus-off recovery (test 1)	20511001.TST	PASS	
3.5.11	Bus-off recovery (test 2)	20511002.TST	PASS	
3.5.12	Completion condition for passive-error flag	20512000.TST	PASS	
3.5.13	Form error in passive-error delimiter (2nd bit)	20513001.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.5.13	Form error in passive-error delimiter (4th bit)	20513002.TST	PASS	
3.5.13	Form error in passive-error delimiter (7th bit)	20513003.TST	PASS	
3.5.14	Maximum recovery time after corrupted frame	20514000.TST	PASS	
3.5.15	Transition from active to passive error flag (C&S Add-on)	20515001_CS.TST	PASS	C&S Add-on Test
3.6	*Error counter management class*			
3.6.1	TEC increment on bit error during active-error flag (1st bit)	20601001.TST	PASS	
3.6.1	TEC increment on bit error during active-error flag (3rd bit)	20601002.TST	PASS	
3.6.1	TEC increment on bit error during active-error flag (6th bit)	20601003.TST	PASS	
3.6.2	TEC increment on bit error during overload flag (1st Bit)	20602001.TST	PASS	
3.6.2	TEC increment on bit error during overload flag (4th Bit)	20602002.TST	PASS	
3.6.2	TEC increment on bit error during overload flag (6th Bit)	20602003.TST	PASS	
3.6.3	TEC increment when active-error flag followed by dominant bits	20603000.TST	PASS	
3.6.4	TEC increment when passive-error flag followed by dominant bits	20604000.TST	PASS	
3.6.4	TEC non increment when passive-error flag overwritten by up to 13 dominant bits (2nd bit - C&S Add-on)	20604001_CS.TST	PASS	C&S Add-on Test
3.6.4	TEC non increment when passive-error flag overwritten by up to 13 dominant bits (1st bit - C&S Add-on)	20604002_CS.TST	PASS	C&S Add-on Test
3.6.4	TEC increment when passive-error flag overwritten by 14 dominant bits (1st bit - C&S Add-on)	20604003_CS.TST	PASS	C&S Add-on Test
3.6.4	TEC increment when passive-error flag overwritten by 14 dominant bits (2nd bit - C&S Add-on)	20604004_CS.TST	PASS	C&S Add-on Test
3.6.4	TEC non increment when passive-error flag overwritten by up to 13 dominant bits (5th bit - C&S Add-on)	20604005_CS.TST	PASS	C&S Add-on Test
3.6.5	TEC increment when overload flag is followed by dominant bits	20605000.TST	PASS	
3.6.6	TEC increment on bit error in data frame (SOF)	20606001.TST	PASS	
3.6.6	TEC increment on bit error in data frame (ID)	20606002.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.6.6	TEC increment on bit error in data frame (CRC)	20606003.TST	PASS	
3.6.6	TEC increment on bit error in data frame (DLC)	20606004.TST	PASS	
3.6.6	TEC increment on bit error in data frame (Data)	20606005.TST	PASS	
3.6.6	TEC increment on bit error in data frame (Data - C&S Add-on)	20606006_CS.TST	PASS	C&S Add-on Test
3.6.6	TEC increment on bit error in data frame (CRC - C&S Add-on)	20606007_CS.TST	PASS	C&S Add-on Test
3.6.6	TEC increment on bit error in data frame (IDE - C&S Add-on)	20606008_CS.TST	PASS	C&S Add-on Test
3.6.7	TEC increment on form error in a frame (in CRC)	20607001.TST	PASS	
3.6.7	TEC increment on form error in a frame (in ACK_DEL)	20607002.TST	PASS	
3.6.7	TEC increment on form error in a frame (in 1st bit of EOF)	20607003.TST	PASS	
3.6.7	TEC increment on form error in a frame (in 4th bit of EOF)	20607004.TST	PASS	
3.6.7	TEC increment on form error in a frame (in 7th bit of EOF)	20607005.TST	PASS	
3.6.8	TEC increment on acknowledgement error	20608000.TST	PASS	
3.6.9	TEC increment on form error in error delimiter (2nd bit)	20609001.TST	PASS	
3.6.9	TEC increment on form error in error delimiter (4th bit)	20609002.TST	PASS	
3.6.9	TEC increment on form error in error delimiter (6th bit)	20609003.TST	PASS	
3.6.9	TEC increment on form error in error delimiter (7th bit)	20609004_cs.TST	PASS	
3.6.10	TEC increment on form error in overload delimiter (2nd bit)	20610001.TST	PASS	
3.6.10	TEC increment on form error in overload delimiter (7th bit)	20610002.TST	PASS	
3.6.11	TEC decrement on successful frame transmission for TEC<128	20611000.TST	PASS	
3.6.12	TEC decrement on successful frame transmission for TEC>127	20612000.TST	PASS	
3.6.13	TEC non-increment on 13 bit long overload flag	20613000.TST	PASS	
3.6.14	TEC non-increment on 13 bit long error flag	20614000.TST	PASS	
3.6.15	TEC non-increment on form error at last bit of overload delimiter	20615000.TST	PASS	
3.6.16	TEC non-increment on form error at last bit of error delimiter	20616000.TST	PASS	

Ref.	Description	Test script	Result	Comment
3.6.17	TEC non-incremented on acknowledgement error in passive state	20617000.TST	PASS	
3.6.18	TEC increment on acknowledgement error in passive state	20618000.TST	PASS	
3.6.19	TEC non-increment on stuff error during arbitration	20619000.TST	PASS	
3.6.19	TEC non-increment on stuff error during arbitration and increment on other error condition	20619001_CS.tst	PASS	C&S Add-on Test
3.6.20	TEC non-decrement on reception	20620000_CS.TST	PASS	C&S Add-on Test
3.6.20	TEC non-decrement on reception and no TEC increment on reception error (Arb. lost)	20620001_CS.TST	PASS	C&S Add-on Test
3.7.	*Bit timing class*			*See:* Generation of Bit Timing Test Atoms
4	**Bi-directional frame type**			
4.1.1	Receive standard remote frame and number of data (DLC 0 - C&S Add-on)	30101001_CS.TST	PASS	C&S Add-on Test
4.1.1	Receive standard remote frame and number of data (DLC 1 - C&S Add-on)	30101002_CS.TST	PASS	C&S Add-on Test
4.1.1	Receive standard remote frame and number of data (DLC 2 - C&S Add-on)	30101003_CS.TST	PASS	C&S Add-on Test
4.1.1	Receive standard remote frame and number of data (DLC 3 - C&S Add-on)	30101004_CS.TST	PASS	C&S Add-on Test
4.1.1	Receive standard remote frame and number of data (DLC 4 - C&S Add-on)	30101005_CS.TST	PASS	C&S Add-on Test
4.1.1	Receive standard remote frame and number of data (DLC 5 - C&S Add-on)	30101006_CS.TST	PASS	C&S Add-on Test
4.1.1	Receive standard remote frame and number of data (DLC 6 - C&S Add-on)	30101007_CS.TST	PASS	C&S Add-on Test
4.1.1	Receive standard remote frame and number of data (DLC 7 - C&S Add-on)	30101008_CS.TST	PASS	C&S Add-on Test
4.1.1	Receive standard remote frame and number of data (DLC 8 - C&S Add-on)	30101009_CS.TST	PASS	C&S Add-on Test
4.1.2	Receive extended remote frame and number of data (DLC 0 - C&S Add-on)	30102001_CS.TST	PASS	C&S Add-on Test
4.1.2	Receive extended remote frame and number of data (DLC 1 - C&S Add-on)	30102002_CS.TST	PASS	C&S Add-on Test
4.1.2	Receive extended remote frame and number of data (DLC 2 - C&S Add-on)	30102003_CS.TST	PASS	C&S Add-on Test
4.1.2	Receive extended remote frame and number of data (DLC 3 - C&S Add-on)	30102004_CS.TST	PASS	C&S Add-on Test
4.1.2	Receive extended remote frame and number of data (DLC 4 - C&S Add-on)	30102005_CS.TST	PASS	C&S Add-on Test

Ref.	Description	Test script	Result	Comment
4.1.2	Receive extended remote frame and number of data (DLC 5 - C&S Add-on)	30102006_CS.TST	PASS	C&S Add-on Test
4.1.2	Receive extended remote frame and number of data (DLC 6 - C&S Add-on)	30102007_CS.TST	PASS	C&S Add-on Test
4.1.2	Receive extended remote frame and number of data (DLC 7 - C&S Add-on)	30102008_CS.TST	PASS	C&S Add-on Test
4.1.2	Receive extended remote frame and number of data (DLC 8 - C&S Add-on)	30102009_CS.TST	PASS	C&S Add-on Test
4.1.3	Receive standard remote frame DLC greater than 8 (DLC 9 - C&S Add-on)	30103001_CS.TST	PASS	C&S Add-on Test
4.1.3	Receive standard remote frame DLC greater than 8 (DLC 10 - C&S Add-on)	30103002_CS.TST	PASS	C&S Add-on Test
4.1.3	Receive standard remote frame DLC greater than 8 (DLC 11 - C&S Add-on)	30103003_CS.TST	PASS	C&S Add-on Test
4.1.3	Receive standard remote frame DLC greater than 8 (DLC 12 - C&S Add-on)	30103004_CS.TST	PASS	C&S Add-on Test
4.1.3	Receive standard remote frame DLC greater than 8 (DLC 13 - C&S Add-on)	30103005_CS.TST	PASS	C&S Add-on Test
4.1.3	Receive standard remote frame DLC greater than 8 (DLC 14 - C&S Add-on)	30103006_CS.TST	PASS	C&S Add-on Test
4.1.3	Receive standard remote frame DLC greater than 8 (DLC 15 - C&S Add-on)	30103007_CS.TST	PASS	C&S Add-on Test
4.1.4	Transmit standard remote frame and number of data (DLC 0 - C&S Add-on)	30104001_CS.TST	PASS	C&S Add-on Test
4.1.4	Transmit standard remote frame and number of data (DLC 1 - C&S Add-on)	30104002_CS.TST	PASS	C&S Add-on Test
4.1.4	Transmit standard remote frame and number of data (DLC 2 - C&S Add-on)	30104003_CS.TST	PASS	C&S Add-on Test
4.1.4	Transmit standard remote frame and number of data (DLC 3 - C&S Add-on)	30104004_CS.TST	PASS	C&S Add-on Test
4.1.4	Transmit standard remote frame and number of data (DLC 4 - C&S Add-on)	30104005_CS.TST	PASS	C&S Add-on Test
4.1.4	Transmit standard remote frame and number of data (DLC 5 - C&S Add-on)	30104006_CS.TST	PASS	C&S Add-on Test
4.1.4	Transmit standard remote frame and number of data (DLC 6 - C&S Add-on)	30104007_CS.TST	PASS	C&S Add-on Test
4.1.4	Transmit standard remote frame and number of data (DLC 7 - C&S Add-on)	30104008_CS.TST	PASS	C&S Add-on Test
4.1.4	Transmit standard remote frame and number of data (DLC 8 - C&S Add-on)	30104009_CS.TST	PASS	C&S Add-on Test
4.1.5	Transmit extended remote frame and number of data (DLC 0 - C&S Add-on)	30105001_CS.TST	PASS	C&S Add-on Test
4.1.5	Transmit extended remote frame and number of data (DLC 1 - C&S Add-on)	30105002_CS.TST	PASS	C&S Add-on Test
4.1.5	Transmit extended remote frame and number of data (DLC 2 - C&S Add-on)	30105003_CS.TST	PASS	C&S Add-on Test
4.1.5	Transmit extended remote frame and number of data (DLC 3 - C&S Add-on)	30105004_CS.TST	PASS	C&S Add-on Test

Ref.	Description	Test script	Result	Comment
4.1.5	Transmit extended remote frame and number of data (DLC 4 - C&S Add-on)	30105005_CS.TST	PASS	C&S Add-on Test
4.1.5	Transmit extended remote frame and number of data (DLC 5 - C&S Add-on)	30105006_CS.TST	PASS	C&S Add-on Test
4.1.5	Transmit extended remote frame and number of data (DLC 6 - C&S Add-on)	30105007_CS.TST	PASS	C&S Add-on Test
4.1.5	Transmit extended remote frame and number of data (DLC 7 - C&S Add-on)	30105008_CS.TST	PASS	C&S Add-on Test
4.1.5	Transmit extended remote frame and number of data (DLC 8 - C&S Add-on)	30105009_CS.TST	PASS	C&S Add-on Test
4.1.6	Transmit standard remote frame DLC greater than 8 (DLC 9 - C&S Add-on)	30106001_CS.TST	PASS	C&S Add-on Test
4.1.6	Transmit standard remote frame DLC greater than 8 (DLC 10 - C&S Add-on)	30106002_CS.TST	PASS	C&S Add-on Test
4.1.6	Transmit standard remote frame DLC greater than 8 (DLC 11 - C&S Add-on)	30106003_CS.TST	PASS	C&S Add-on Test
4.1.6	Transmit standard remote frame DLC greater than 8 (DLC 12 - C&S Add-on)	30106004_CS.TST	PASS	C&S Add-on Test
4.1.6	Transmit standard remote frame DLC greater than 8 (DLC 13 - C&S Add-on)	30106005_CS.TST	PASS	C&S Add-on Test
4.1.6	Transmit standard remote frame DLC greater than 8 (DLC 14 - C&S Add-on)	30106006_CS.TST	PASS	C&S Add-on Test
4.1.6	Transmit standard remote frame DLC greater than 8 (DLC 15 - C&S Add-on)	30106007_CS.TST	PASS	C&S Add-on Test
4.1.7	Arbitration in standard remote frame (C&S Add-on)	30107000_CS.TST	PASS	C&S Add-on Test
4.1.7.1	Arbitration in standard remote frame (C&S Add-on) (check arbitration winning frame)	30107001_CS.TST	PASS	C&S Add-on Test
4.1.8	Arbitration in extended remote frame (C&S Add-on)	30108000_CS.TST	PASS	C&S Add-on Test
4.1.8.1	Arbitration in extended remote frame (C&S Add-on) (check arbitration winning frame)	30108001_CS.TST	PASS	C&S Add-on Test
4.13	*Error counter management class*			
4.13.1	REC unaffected when incr. TEC	30601000.TST	PASS	
4.13.1	REC unaffected when incr. TEC	30601001_CS.TST	PASS	C&S Add-on Test
4.13.2	TEC unaffected when incr. REC	30602000.TST	PASS	
4.13.2	TEC unaffected when incr. REC	30602001_CS.TST	PASS	C&S Add-on Test

6.1 Bit Timing Tests

Generation of Bit Timing Test Atoms

To reduce the execution time of the bit timing test suite, a limited number of configurations are tested instead of the whole possible spectrum. These configurations represent the most critical timing settings where errors can occur. In the past it was recognized that when errors are present, they can be found with these configurations. If an error comes across with these settings, the configuration is expanded to isolate the error. If the chip passes these tests, the other possible timing settings shall be “pass” too.

Bit Timing Configurations:

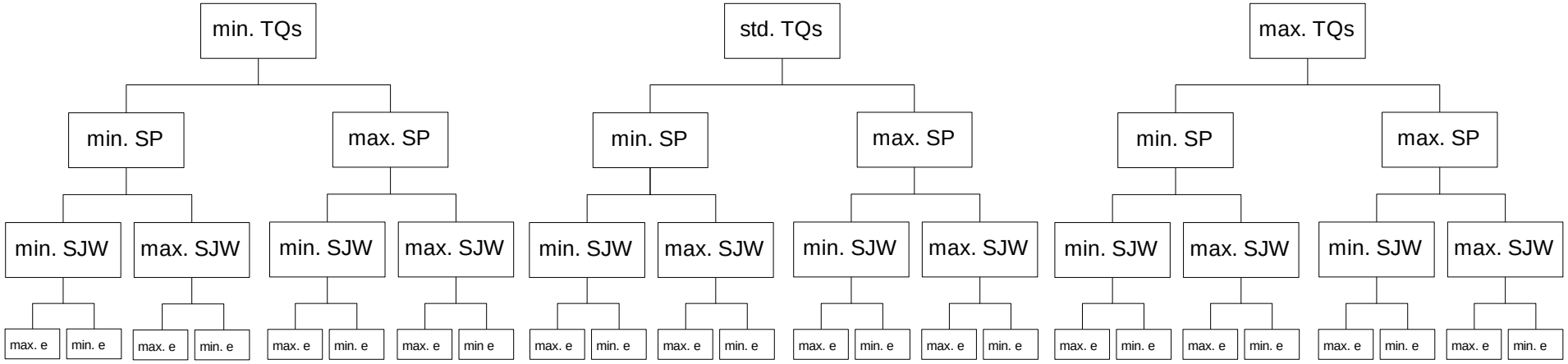


Figure 1

References:

std / min / max TQs: The standard, minimal and maximal number of Time Quanta per Bit Time.
min / max SP: The minimal and maximal Sample Point possible configuration.
min / max SJW: The minimal and maximal Resynchronization Jump Width.
min / max e: The minimal and maximal phase error "e". This is used only in the synchronization and glitch tests.

Standard Time Quanta:
Configuration of NTQs and BRP for optimal minimal and maximal Sample Point settings.

Maximal Time Quanta:
Maximal number of Time Quanta per Bit-Time (if possible also a low BRP). The result of this configuration is the test of the bit timing in a critical state (very short time quanta). In this configuration, the delay time of the real CAN node is considered.

Minimal Time Quanta:
Minimal number of Time Quanta and a normal BRP. In this configuration the lowest possible settings will be tested.

Tested Configurations:

Configuration Table for Bit Timing Tests with BRP=1 12 Mhz CAN		
	BRP	1
	TQ	24
max. TQ:	Baud rate (KBit)	500
	BRP	1
	TQ	15
std. TQ:	Baud rate (KBit)	800
	BRP	1
	TQ	12
min. TQ:	Baud rate (KBit)	1000

Configuration Table for Bit Timing Tests with BRP=3 12 Mhz CAN		
	BRP	3
	TQ	25
max. TQ:	Baud rate (KBit)	160
	BRP	3
	TQ	16
std. TQ:	Baud rate (KBit)	250
	BRP	3
	TQ	8
min. TQ:	Baud rate (KBit)	500

Configuration Table for Bit Timing Tests with BRP=4 12 Mhz CAN		
	BRP	4
	TQ	24
max. TQ:	Baud rate (KBit)	125
	BRP	4
	TQ	15
std. TQ:	Baud rate (KBit)	200
	BRP	4
	TQ	9
min. TQ:	Baud rate (KBit)	333

Configuration Table for Bit Timing Tests with BRP=2 12 Mhz CAN		
	BRP	2
	TQ	24
max. TQ:	Baud rate (KBit)	250
	BRP	2
	TQ	15
std. TQ:	Baud rate (KBit)	400
	BRP	2
	TQ	12
min. TQ:	Baud rate (KBit)	500

Table 1

6.1.1 Bit timing Tests Lists – BRP 1

Ref.	Description	Verdict max. TQ	Verdict std. TQ	Verdict min. TQ	Comment
2.7	**Receiver**				
2.7.1	Sample point test	PASS	PASS	PASS	
2.7.2	Hard synchronization on SOF reception	PASS	PASS	PASS	
2.7.3	Synchronization when e>0 and e≤SJW	PASS	PASS	PASS	
2.7.4	Synchronization when e>0 and e>SJW	PASS	PASS	PASS	
2.7.5	Synchronization when e<0 and |e|≤SJW	PASS	PASS	PASS	
2.7.6	Synchronization when e<0 and |e|>SJW	PASS	PASS	PASS	
2.7.7	Glitch filtering test on positive phase error	PASS	PASS	PASS	
2.7.8	Glitch filtering test on negative phase error	PASS	PASS	PASS	
2.7.9	Glitch filtering during bus idle	PASS	PASS	PASS	
2.7.9_CS	Glitch filtering during bus idle (C&S)	PASS	PASS	PASS	C&S Add-on Test
2.7.10	Non-Resynchronization after a dominant sampled bit	PASS	PASS	PASS	
2.7.11_CS	Synchronization for e > 0 and e > SJW in first bit of intermission field after successful reception	EXEC	EXEC	EXEC	C&S Add-on Test Execute only

3.7	Transmitter				
3.7.1	Sample Point Test	PASS	PASS	PASS	
3.7.2	Hard Synchronization on SOF Reception before sample point	PASS	PASS	PASS	
3.7.3	Hard Synchronization on SOF Reception after sample point	PASS	PASS	PASS	
3.7.4	Synchronization when e < 0 and |e| ≤ SJW	PASS	PASS	PASS	
3.7.5	Synchronization for e < 0 and |e| > SJW	PASS	PASS	PASS	Refer to remark
3.7.6	Glitch filtering test on negative phase error	PASS	PASS	PASS	
3.7.7	Non-synchronization on dominant bit transmission	PASS	PASS	PASS	
3.7.8	Synchronization before information processing time	PASS	PASS	PASS	Refer to remark
3.7.9	Synchronization after sample point while sending a dominant bit	--	--	--	
3.7.10_CS	Synchronization for e > 0 and e > SJW in first bit of intermission field after successful transmission	EXEC	EXEC	EXEC	C&S Add-on Test Execute only

6.1.2 Bit timing Tests Lists – BRP 2

Ref.	Description	Verdict max. TQ	Verdict std. TQ	Verdict min. TQ	Comment
2.7	**Receiver**				
2.7.1	Sample point test	PASS	PASS	PASS	
2.7.2	Hard synchronization on SOF reception	PASS	PASS	PASS	
2.7.3	Synchronization when e>0 and e≤SJW	PASS	PASS	PASS	
2.7.4	Synchronization when e>0 and e>SJW	PASS	PASS	PASS	
2.7.5	Synchronization when e<0 and |e|≤SJW	PASS	PASS	PASS	
2.7.6	Synchronization when e<0 and |e|>SJW	PASS	PASS	PASS	
2.7.7	Glitch filtering test on positive phase error	PASS	PASS	PASS	
2.7.8	Glitch filtering test on negative phase error	PASS	PASS	PASS	
2.7.9	Glitch filtering during bus idle	PASS	PASS	PASS	
2.7.9_CS	Glitch filtering during bus idle (C&S)	PASS	PASS	PASS	C&S Add-on Test
2.7.10	Non-Resynchronization after a dominant sampled bit	PASS	PASS	PASS	
2.7.11_CS	Synchronization for e > 0 and e > SJW in first bit of intermission field after successful reception	EXEC	EXEC	EXEC	C&S Add-on Test Execute only

3.7	Transmitter				
3.7.1	Sample Point Test	PASS	PASS	PASS	
3.7.2	Hard Synchronization on SOF Reception before sample point	PASS	PASS	PASS	
3.7.3	Hard Synchronization on SOF Reception after sample point	PASS	PASS	PASS	
3.7.4	Synchronization when e < 0 and |e| ≤ SJW	PASS	PASS	PASS	
3.7.5	Synchronization for e < 0 and |e| > SJW	PASS	PASS	PASS	Refer to remark
3.7.6	Glitch filtering test on negative phase error	PASS	PASS	PASS	
3.7.7	Non-synchronization on dominant bit transmission	PASS	PASS	PASS	
3.7.8	Synchronization before information processing time	PASS	PASS	PASS	Refer to remark
3.7.9	Synchronization after sample point while sending a dominant bit	--	--	--	
3.7.10_CS	Synchronization for e > 0 and e > SJW in first bit of intermission field after successful transmission	EXEC	EXEC	EXEC	C&S Add-on Test Execute only

6.1.3 Bit timing Tests Lists – BRP 3

Ref.	Description	Verdict max. TQ	Verdict std. TQ	Verdict min. TQ	Comment
2.7	**Receiver**				
2.7.1	Sample point test	PASS	PASS	PASS	
2.7.2	Hard synchronization on SOF reception	PASS	PASS	PASS	
2.7.3	Synchronization when e>0 and e≤SJW	PASS	PASS	PASS	
2.7.4	Synchronization when e>0 and e>SJW	PASS	PASS	PASS	
2.7.5	Synchronization when e<0 and |e|≤SJW	PASS	PASS	PASS	
2.7.6	Synchronization when e<0 and |e|>SJW	PASS	PASS	PASS	
2.7.7	Glitch filtering test on positive phase error	PASS	PASS	PASS	
2.7.8	Glitch filtering test on negative phase error	PASS	PASS	PASS	
2.7.9	Glitch filtering during bus idle	PASS	PASS	PASS	
2.7.9_CS	Glitch filtering during bus idle (C&S)	PASS	PASS	PASS	C&S Add-on Test
2.7.10	Non-Resynchronization after a dominant sampled bit	PASS	PASS	PASS	
2.7.11_CS	Synchronization for e > 0 and e > SJW in first bit of intermission field after successful reception	EXEC	EXEC	EXEC	C&S Add-on Test execute only

3.7	Transmitter				
3.7.1	Sample Point Test	PASS	PASS	PASS	
3.7.2	Hard Synchronization on SOF Reception before sample point	PASS	PASS	PASS	
3.7.3	Hard Synchronization on SOF Reception after sample point	PASS	PASS	PASS	
3.7.4	Synchronization when e < 0 and |e| ≤ SJW	PASS	PASS	PASS	
3.7.5	Synchronization for e < 0 and |e| > SJW	PASS	PASS	PASS *	Refer to remark
3.7.6	Glitch filtering test on negative phase error	PASS	PASS	PASS	
3.7.7	Non-synchronization on dominant bit transmission	PASS	PASS	PASS	
3.7.8	Synchronization before information processing time	PASS	PASS	PASS	Refer to remark
3.7.9	Synchronization after sample point while sending a dominant bit	--	--	--	
3.7.10_CS	Synchronization for e > 0 and e > SJW in first bit of intermission field after successful transmission	EXEC	EXEC	EXEC	C&S Add-on Test execute only

*Test 3.7.5 at MIN TQ is performed at 400K with nTQ = 10; BRP = 3

6.1.4 Bit timing Tests Lists – BRP 4

Ref.	Description	Verdict max. TQ	Verdict std. TQ	Verdict min. TQ	Comment
2.7	**Receiver**				
2.7.1	Sample point test	PASS	PASS	PASS	
2.7.2	Hard synchronization on SOF reception	PASS	PASS	PASS	
2.7.3	Synchronization when e>0 and e≤SJW	PASS	PASS	PASS	
2.7.4	Synchronization when e>0 and e>SJW	PASS	PASS	PASS	
2.7.5	Synchronization when e<0 and |e|≤SJW	PASS	PASS	PASS	
2.7.6	Synchronization when e<0 and |e|>SJW	PASS	PASS	PASS	
2.7.7	Glitch filtering test on positive phase error	PASS	PASS	PASS	
2.7.8	Glitch filtering test on negative phase error	PASS	PASS	PASS	
2.7.9	Glitch filtering during bus idle	PASS	PASS	PASS	
2.7.9_CS	Glitch filtering during bus idle (C&S)	PASS	PASS	PASS	C&S Add-on Test
2.7.10	Non-Resynchronization after a dominant sampled bit	PASS	PASS	PASS	
2.7.11_CS	Synchronization for e > 0 and e > SJW in first bit of intermission field after successful reception	EXEC	EXEC	EXEC	C&S Add-on Test execute only

3.7	Transmitter				
3.7.1	Sample Point Test	PASS	PASS	PASS	
3.7.2	Hard Synchronization on SOF Reception before sample point	PASS	PASS	PASS	
3.7.3	Hard Synchronization on SOF Reception after sample point	PASS	PASS	PASS	
3.7.4	Synchronization when e < 0 and |e| ≤ SJW	PASS	PASS	PASS	
3.7.5	Synchronization for e < 0 and |e| > SJW	PASS	PASS	--	Refer to remark
3.7.6	Glitch filtering test on negative phase error	PASS	PASS	PASS	
3.7.7	Non-synchronization on dominant bit transmission	PASS	PASS	PASS	
3.7.8	Synchronization before information processing time	PASS	PASS	PASS	Refer to remark
3.7.9	Synchronization after sample point while sending a dominant bit	--	--	--	
3.7.10_CS	Synchronization for e > 0 and e > SJW in first bit of intermission field after successful transmission	EXEC	EXEC	EXEC	C&S Add-on Test execute only

7 Test Protocol of “Exec. only” tests

“Exec. Only” Tests means test cases which are designed to show the behaviour of the IUT but not to find a verdict about the behaviour. The tests are based on not in detail described protocol rules, so different implementations may behave in different ways.

Test case 20508001 C&S Add on Data link layer Test class

TEST: 3.5.8.1 Purpose and limits of this Test Case

CAN_VERSION ∈ {A, B, BP}

The purpose of this test is to verify that a Passive State IUT is able to transmit a frame starting with an identifier and without transmitting SOF, when detecting a Dominant bit on the 3rd bit of the Intermission field in case it is receiver of the previous message.

State	Description
Set-Up	The IUT is set to the TEC Passive State.
Test	The LT causes the IUT to transmit 1 frames. The LT lets the IUT loose arbitration. This frame must end with EOF Field followed by the Intermission Field. At the second bit of the Intermission Field, the LT starts sending a frame with the same Frame ID and Data (normally forbidden by rules for network configuration).
Verification	The IUT should start the transmission without SOF and arbitrate against the frame sent by the LT.
Reference	ISO 11898 Section 10.4.2.2 SOF
Notes	

Excerpt of ISO11898-1

10.4.2.2 SOF

SOF shall mark the beginning of data and remote frames. It shall consist of a single dominant bit.

A node shall send a SOF only when the bus is idle (see 10.4.6.3). A node sampling a dominant bit during suspend transmission or at the third bit of intermission shall accept it as SOF.

If a node has a pending transmission that is error-active or which has been the receiver of the previous frame samples, a dominant bit at the third bit of intermission shall, with the next bit, start transmitting its message with the first bit of its identifier without first transmitting a SOF bit and without becoming the receiver.

All nodes shall synchronize to the leading edge caused by SOF of the node starting transmission first.

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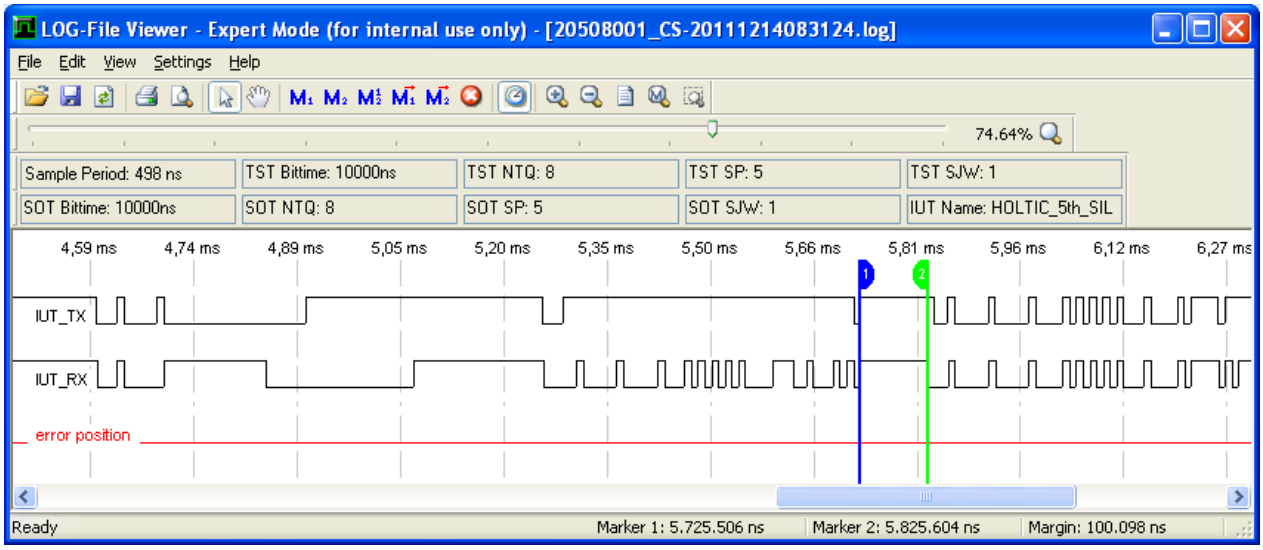
Picture of the described scenario:



Margin between Marker 1 and Marker 2: 100.098ns ≙ 10Bit

The Lower Tester inverts a recessive stuff Bit of the ID field of the IUT acting as transmitter (see picture). The IUT is forced to error passive by additional errors. The Lower Tester sends two messages. The IUT confirm these messages by acknowledge and shall send out its Tx- message disturbed by the error scenario without Suspend transmission time. The LT force the 3rd bit of intermission to dominant to force the IUT to start transmit its frame without SOF Bit.

Observation:

The IUT is able to send its message without SOF in this particular situation.

Test case 20508002 C&S Add on Data link layer Test class

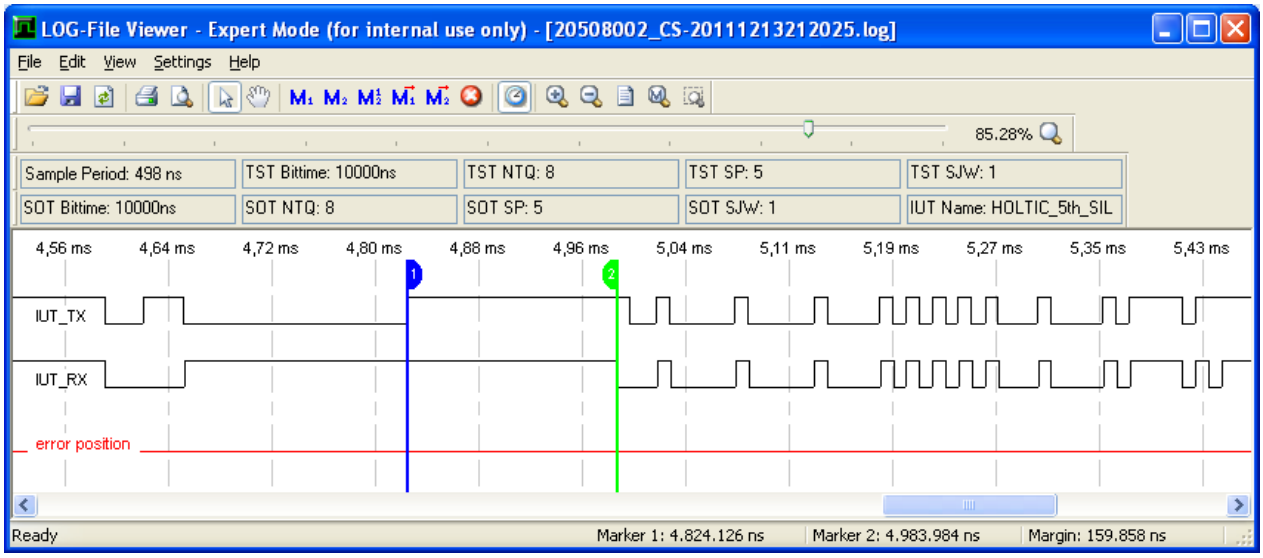
TEST: 3.5.8.2-3 Purpose and limits of this Test Case

CAN_VERSION ∈ {A, B, BP}

The purpose of this test is to verify that a Passive State IUT transmit is able to transmit a frame starting with an identifier and without transmitting SOF, when detecting a Dominant bit on the 3rd bit of the Intermission Field in case it is receiver state because of the previous frame arbitration lost.

State	Description
Set-Up	No action required. The IUT is left in the Default State.
Test	The LT causes the IUT to transmit 1 frames. The IUT is set to the REC Passive State because the LT lets the IUT loose arbitration followed by an error scenario to force REC passive. This passive error frame must end with EOF Field followed by the Intermission Field. At the second bit of the Intermission Field, the LT starts sending a frame with the same Frame ID and Data. (normally forbidden by rules for network configuration)
Verification	The IUT should start the transmission without SOF and arbitrate against the frame sent by the LT.
Reference	ISO 11898 Section 10.4.2.2 SOF
Notes	The definition of “receiver of previous Frame” could be interpreted as “being in receive mode before next transmission”

Picture of the described scenario 3.5.8.2:



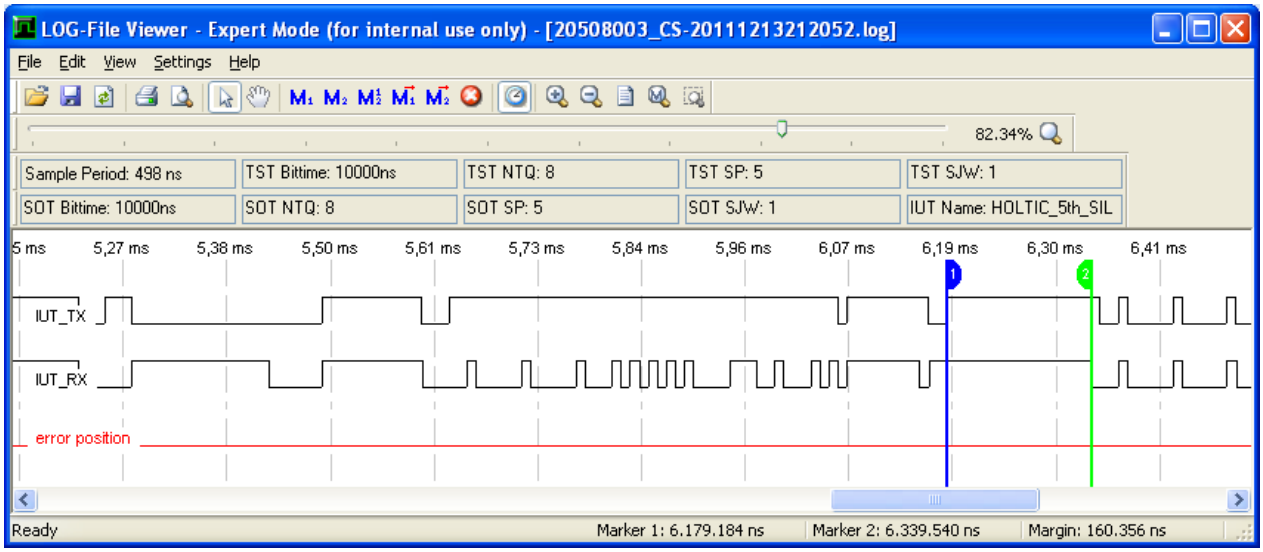
Margin between Marker 1 and Marker 2: 159.858ns ≙ 16Bit

The Lower Tester force an arbitration lost into one Bit of the ID field of the IUT acting as transmitter (see picture). After being receiver of the higher prior message ID the IUT is forced to error passive by additional errors. The IUT shall send out its Tx- message disturbed by the Arbitration lost scenario without Suspend transmission time. The LT force the 3rd bit of intermission to dominant to force the IUT to start transmit its frame without SOF Bit.

Observation:

The IUT is able to send its message without SOF in this particular situation.

Picture of the described scenario 3.5.8.3:



Margin between Marker 1 and Marker 2: 160.356ns ≙ 16Bit

The Lower Tester force an arbitration lost into one Bit of the ID field of the IUT acting as transmitter (see picture). After being receiver of the higher prior message ID the IUT is forced to error passive by additional errors. The IUT shall send out its Tx- message disturbed by the Arbitration lost scenario and will be receiver of a valid message. After that an overload condition followed by an additional error will set the IUT to REC-passive state. The IUT shall send out its Tx- message without Suspend transmission time. The LT force the 3rd bit of intermission to dominant to force the IUT to start transmit its frame without SOF Bit.

Observation:

The IUT is able to send its message without SOF in this particular situation.

Test case 17011 C&S Add on Test Bit timing class*

TEST: 2.7.11 Synchronisation for e > 0 and e > SJW in first bit of intermission field after successful transmission (C&S)

Purpose and limits of this Test Case

CAN_VERSION ∈ {A, B, BP}

The purpose of this test is to verify the behaviour of an IUT acting as a receiver detecting a positive phase error “e” on a Recessive to Dominant edge inserted into the intermission bit 1 with e > SJW.

The values tested for “e” are measured in Time Quanta with
e ∈ [(SJW + 1), (NTQ – (TSEG2 + 1))].

There is one Elementary Test to perform for each possible value of e.

C&S did the test twice, with BRP = 1 and BRP >=2. (typical value is 4)

Test Case organisation

State	Description
Set-Up	No action required, the IUT is left in the Default State.
Test	The LT generates a dominant Bit within the first bit of intermission. The recessive to dominant edge (start of bit) is delayed by an amount of “e” time quanta and shortens the same bit by an amount of e - SJW.
Verification	The IUT should generate an Overload Frame 1 bit time – (e – SJW) time quanta after the Recessive to Dominant edge of the delayed dominant Bit (disturbance in intermission 1 bit).
Reference	ISO11898 12.4.2.1 C) Hard synchronization is performed during interframe space (with the exception of the first bit of intermission) whenever there is a »recessive« to »dominant« edge.
Notes	In case the overload frame starts exact one bit time after the falling edge on RX it could be a hard synchronisation.

Excerpt of ISO11898-1

12.4.2 Synchronization

12.4.2.1 Description

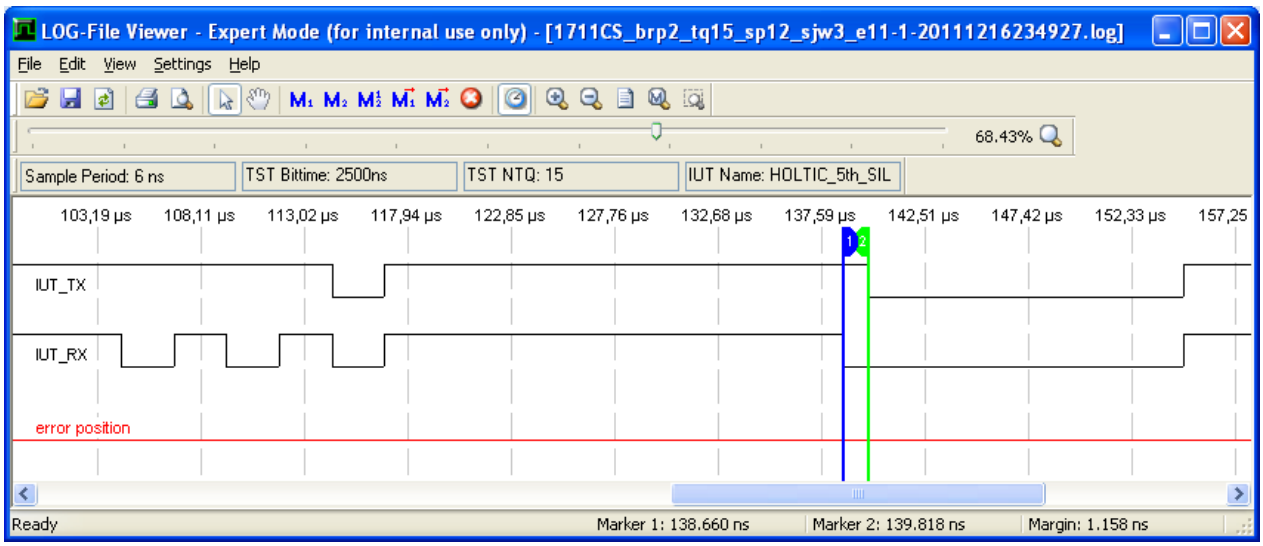
Hard synchronization and resynchronization shall be two forms of synchronization. They shall obey the following rules.

a) Only one synchronization within one bit time (between two sample points) shall be allowed.

b) A recessive to dominant edge shall be used for synchronization only if the bus state detected at the previous sample point (previous read bus state) differs from the bus state immediately after the edge.

c) Hard synchronization shall be performed during interframe space (with the exception of the first bit of intermission) whenever there is a recessive to dominant edge.

Example Picture of the described scenario:



Margin between Marker 1 and Marker 2: 1158ns ≙ 0,46 Bit

We cause a falling edge within the first bit of intermission to set a dominant bit and check if the following overload frame start according soft sync rules +- a possible tolerance because of the 9 bits without a synchronisation.

Observation:

The CAN implementation is able to do a soft synchronisation at first bit of intermission.

Test case 27010 C&S Add on Test Bit timing class*

TEST: 3.7.10 Synchronisation for e > 0 and e > SJW in first bit of intermission field after successful transmission (C&S Add-on)

Purpose and limits of this Test Case

CAN_VERSION ∈ {A, B, BP}

The purpose of this test is to verify the behaviour of an IUT acting as a receiver detecting a positive phase error e on a Recessive to Dominant edge inserted into the intermission bit 1 with e > SJW.

Second test purpose is to check the correct behaviour (being receiver) after being transmitter of the previous frame.

The values tested for e are measured in Time Quanta with
e ∈ [(SJW + 1), (NTQ – (TSEG2 + 1))].

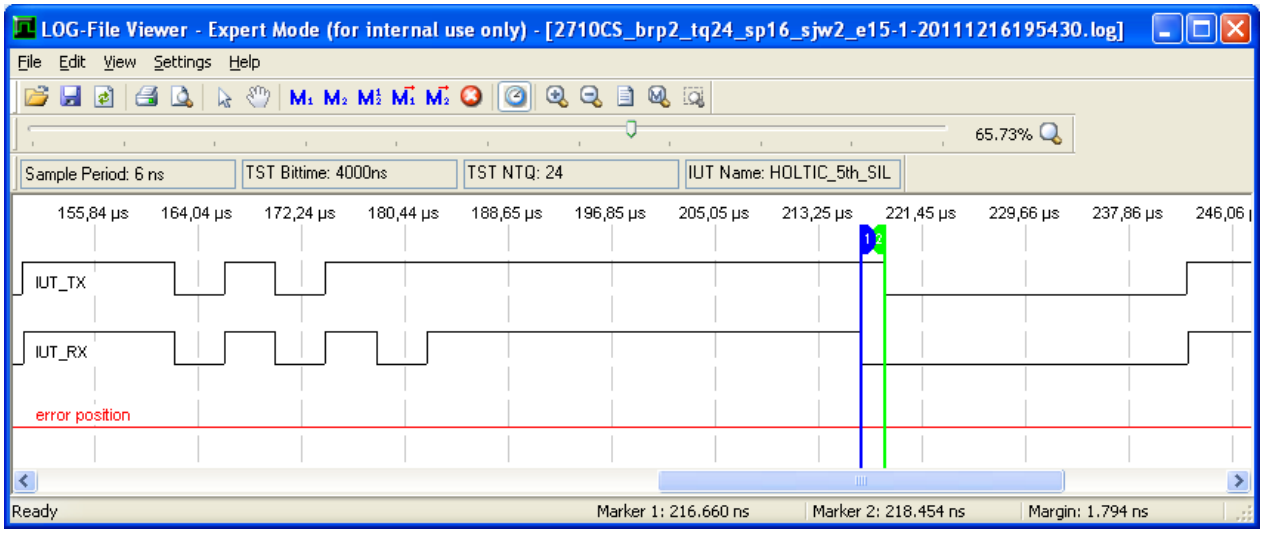
There is one Elementary Test to perform for each possible value of e.

C&S did the test twice, with BRP = 1 and BRP >=2.

Test Case organisation

State	Description
Set-Up	No action required. The IUT is left in the Default State.
Test	The LT generates a dominant Bit within the first bit of intermission. The recessive to dominant edge (start of bit) is delayed by an amount of e time quanta and shortens the same bit by an amount of e - SJW.
Verification	The IUT should generate an Overload Frame 1 bit time – (e – SJW) time quanta after the Recessive to Dominant edge of the delayed dominant Bit (disturbance in intermission 1 bit).
Reference	ISO11898 12.4.2.1 C) Hard synchronization is performed during interframe space (with the exception of the first bit of intermission) whenever there is a »recessive« to »dominant« edge.
Notes	In case the overload frame starts exact one bit time after the falling edge on RX it could be a hard synchronisation.

Example Picture of the described scenario:



Margin between Marker 1 and Marker 2: 1794ns ≙ 0,45 Bit !

We cause a falling edge within the first bit of intermission to set a dominant bit and check if the following overload frame start according soft sync rules +- a possible tolerance because of the 9 bits without a synchronisation.

Observation:

The CAN implementation is able to do a soft synchronisation at first bit of intermission.