Software Porting Guide

HI-6120/21 to Mamba Family Remote Terminal Applications

Devices Supported

HI-6135, HI-6136

HI-6137, HI-6138

August 2016

REVISION HISTORY

Revision	Date	Description of Change
AN-573, Rev. New	08-02-16	Initial Release

Introduction

The Holt Mamba™ family of Integrated Terminals offers customers the World's smallest MIL-STD-1553/1760 solution,providing a complete remote terminal interface between a host processor and MIL-STD-1553 data bus. The Mamba family communicates with the host via a 40MHz 4-wire serial peripheral interface (SPI). For a given device, any combination of the contained MIL STD-1553 functions can be enabled for concurrent operation. The following terminal devices allow users to optimize cost savings by only using the protocol modes they require, while allowing footprint compatible options for future upgradeability.

HI-6135 Remote Terminal

HI-6136 Remote Terminal and Monitor

HI-6137 Remote Terminal and Bus Controller

HI-6138 Remote Terminal, Bus Controller and Monitor

This application note will serve as a software porting guide to help users identify the minor software changes required to easily migrate applications written for HI-6120/21 series Remote Terminals to the new Mamba family.

Overview

The main differences between HI-6120/21 and Mamba Remote Terminals can be summarized as follows:

1. Register Map
    a. Some Register addresses and/or Register Bits have been relocated.
2. Memory Map
    a. Some RAM data structures have different default offset addresses.
    b. Mamba has 8Kx17 SRAM w/ Parity vs. 32Kx16 for HI-6120/21. (Note: RT Applications should never need more than 4K words.)
3. Software Reset Behavior
4. New Feature: MIL-STD-1760 Boot Up Option
5. Interrupts
    a. Additional Registers added to support improved capability
    b. Separated Hardware Interrupts from Remote Terminal Message Interrupts
    c. Interrupt Log Buffer size doubled.
6. SPI interface
    a. Maximum SPI Clock Frequency was increased to 40MHz.
    b. Mamba RT's now have 4 Memory Address Pointer Registers instead of 1 allowing greater flexibility.
    c. Added Fast Access (Direct Addressing) commands for increased register set.

Memory Maps

The Mamba family of terminals support BC/RT/MT operating modes and as such additional configuration registers have been added to support options for the various modes. In addition, the Mamba family has 8Kx17 words of SRAM with Parity vs. the 32Kx16 of the HI-6120/21 family. Therefore, the memory/register map is slightly different for each device family. The reduced RAM should not be a concern for any Remote Terminal application. Any typical RT applications should never need more than 4K words of SRAM. The main RT SRAM data structures are summarized below.

Table 1 - HI-6120/21 vs. Mamba HI-6135/6/7/8 Family Memory Map

Data Structures	Holt HI-6120/21	Holt Mamba HI-6135/6/7/8	Comparison
Registers	0x0000-0x001F	0x0000-0x0051	Mamba has 82 locations vs. 32 locations in HI-6120/21. Only a subset is relevant to RT operation. Some bit locations are different. Interrupt options are enhanced.
Illegalization Table	0x0100-0x01FF	0x0200-0x02FF	Identical usage only the offset is different
Descriptor Table	0x0200-0x03FF	0x0400-0x05FF	Identical usage only the default offset is different
Interrupt Log Buffer	0x0040-0x005F	0x0180-0x01BF	Mamba Family is 64 Words vs. 32 Words for HI-6120/21 allowing a larger history.
RT Temporary Receive Buffer	0x0020-0x003F	0x001C0 - 0x01DF	Identical usage only the offset is different. Optional, not required.
Host Allocated Subaddress Data Buffers	0x0400- 0x7FFF	0x0600-0x1FFF	Identical usage. Offset is different. Mamba has 8Kx17 SRAM. Typical RT applications need less than 4Kx16.

Both HI-6120/21 and Mamba Family Remote Terminal devices support the same user data buffering options. They are Index Mode (Single Buffer), Ping-Pong, Circular Buffer Mode 1 and Circular Buffer Mode 2.

Register Maps

Table 2 below shows the register map comparison between HI-6120/21 and the Mamba RT (HI-6135). The column labeled Mamba Hex Address is the location of the register(s) in the Mamba family that provide the same functionality as the HI-6120/21 registers.

Table 2 - Register Map Comparison HI-6120/21 to Mamba RT HI-6135

Register Number	Hex Address	HI-6120/21 Register Name	Mamba Hex Address	Mamba HI-6135 Register Name
0	0x0000	Configuration Register 1	0x0000/0x0001 0x0017/0x0039	Master Configuration Register
1	0x0001	Configuration Register 2	0x0017/0x0039	Master Status and Reset Register
2	0x0002	Operational Status Register	0x0018	When TEST pin is logic 0, this is “Remote Terminal Current Command Register” When TEST pin is logic 1, this is “Loopback Test Receive Data Register”
3	0x0003	Current Command Register	0x0002	RT Current Control Word Address Register
4	0x0004	Current Control Word Address Register	0x0003	Reserved
5	0x0005	Descriptor Table Base Address Register	0x0019	Reserved
6	0x0006	Pending Interrupt Register	0x0006/0x0009	Hardware Pending Interrupt Register
7	0x0007	1553 Status Word Bits Register	0x001A	Reserved
8	0x0008	Time-Tag Register	0x0049	Reserved
9	0x0009	Interrupt Log Address Register	0x000A	RT Pending Interrupt Status Register
10	0x000A	Current Message Information Word Address Register	0x001B	Interrupt Count and Log Address Register
11-14	0x000B-0x000E	Reserved	N/A	Memory Address Pointer Registers
15	0x000F	Memory Address Pointer (HI-6121 Only)	0x000B-0x000E	Hardware Interrupt Enable Register
16	0x0010	Interrupt Enable Register	0x000F/0x0012 0x0013/0x0016	Reserved
17	0x0011	Time-Tag Utility Register	0x004A	Reserved
18	0x0012	Bus A Select Register	0x001C	RT Interrupt Enable Register

Register Number	Hex Address	HI-6120/21 Register Name	Mamba Hex Address	Mamba HI-6135 Register Name
19	0x0013	Bus B Select Register	0x001D	Hardware Interrupt Output Enable Register
20	0x0014	Built-In Test (BIT) Word Register	0x001E	Reserved
21	0x0015	Alternate Built-In Test (BIT) Word Register	0x001F	Reserved
22	0x0016	Reserved	N/A	RT Interrupt Output Enable Register
23	0x0017	Test Control Register	0x0028	RT Configuration Register
24	0x0018	Loopback Test Transmit Data Register	0x001F	RT Operational Status Register
25	0x0019	Loopback Test Receive Data Register	0x0002	RT Descriptor Table Base Address Register
26-31	0x001A	Reserved	N/A	RT MIL-STD-1553 Status Word Bits Register
27	0x001B	Reserved	N/A	When TEST pin is logic 0, this address is “Remote Terminal Current Message Information Word Register”. When TEST pin is logic 1, this address is “RAM Self-Test Fail Address Register”.
28	0x001C	Reserved	N/A	RT Bus A Select Register
29	0x001D	Reserved	N/A	RT Bus B Select Register
30	0x001E	Reserved	N/A	RT BIT Word Register
31	0x001F	Reserved	N/A	When TEST pin is logic 0, this address is “Remote Terminal Alternate Built-In Test (BIT) Word Register (0x001F)”. When TEST pin is logic 1, this address is “Loopback Test Transmit Data Register (0x001F)”.
32-35	0x0020-0x0023	N/A	N/A	Reserved
36	0x0024	N/A	N/A	When the AUTOEN input pin is logic 1 at rising edge of MR Master Reset and RAM or register initialization failure (RAMIF) occurs, this register is the “Memory Test Fail Address Register”. This register holds the first encountered RAM / register address with data mismatch. There may be others. Once execution starts (or when not using auto-initialization), this register has no function.

Register Number	Hex Address	HI-6120/21 Register Name	Mamba Hex Address	Mamba HI-6135 Register Name
37-39	0x0025-0x0027	N/A	N/A	Reserved
40	0x0028	N/A	N/A	When TEST pin is logic 0, this register has no function. When TEST pin is logic 1, this address is “Self-Test Control Register".
41-56	0x0029-0x0038	N/A	N/A	Reserved
57	0x0039	N/A	N/A	Time Tag Counter Configuration Register
58-72	0x003A-0x0048	N/A	N/A	Reserved
73	0x0049	N/A	N/A	RT Time Tag Counter Register
74	0x004A	N/A	N/A	RT Time Tag Utility Register
75-76	0x004B-0x004C	N/A	N/A	Reserved
77		N/A	N/A	Extended Configuration Register
78		N/A	N/A	Master Configuration Register 2
79-80	0x004F-0x0050	N/A	N/A	Reserved
81	0x0051	N/A	N/A	Checksum Fail Address & EEPROM Lock/Unlock

Register Settings

In general, to configure a remote terminal only requires initializing a handful of registers. The registers themselves and the some of the bit locations are slightly different between HI-6120/21 and Mamba Family, but identifying the needed configuration bits is straightforward.

Table 3 - RT Initialization Register Comparison

Holt HI-6120/21	Holt Mamba HI-6135/6/7/8	Comparison
Configuration Register 1 (0x0000)	Master Configuration Register (0x0000)	See bit descriptions in Datasheet
Configuration Register 2 (0x0001)	RT Configuration Register (0x0017)	See bit descriptions in Datasheet
	Hardware Interrupt Enable Register (0x000F)	Optional: See section on Interrupts
	Hardware Interrupt Output Enable Register (0x0013)	Optional: See section on Interrupts
Interrupt Enable Register (0x0010)	RT Interrupt Enable Register (0x0012)	See section on Interrupts
	RT Output Enable Register (0x0016)	See section on Interrupts
Operation Status Register (0x0002)	RT Operation Status Register (0x0018)	Optional
	Time Tag Counter Configuration Register (0x0039)	For the HI-6120/21 these bits are in Configuration Register 1
Descriptor Table Base Address Register (0x0005)	RT Descriptor Table Base Address Register (0x0017)	Optional

Reset and Initialization

Reset Behavior

For both HI-6120/21 and Mamba family a hardware reset is initiated by asserting the MR Master Reset pin for at least 200ns. The software reset behavior is slightly different. For the HI-6120/21 a software reset is initiated by setting the SRST bit (10) in Configuration Register 1 (0x0000). Software reset has minimal effect on previously initialized registers and RAM structures that define terminal behavior. For the Mamba family, RT software reset is initiated by setting the RTRESET bit (10) in the Master Status and Reset Register (0x0001).

Table 4 - Mamba Family RT Soft Reset Summary

Action	Register Affected
Clears these individual register bits	0x0000 Master Configuration Register, RTSTEX bit 4
	0x0006 Hardware Pending Int Register, RTIP bit 2
	0x0006 Hardware Pending Int Register, RTAPF bit 3
	0x0009 RT Pending Int Register, RT int bits 8 – 3
Clears these entire register addresses	0x0018 RT Operational Status Register
	0x001A RT MIL-STD-1553 Status Word Bits Register
	0x001E RT Built-In Test Word Register
	0x0049 RT Time Tag Counter

Loads these registers from EEPROM if Auto Initialization is Enabled. *These 522 locations comprise the RT1Terminal Checksum stored at 0x01C0 by EECOPY process*	0x000F Hardware Interrupt Enable Register
	0x0012 RT Interrupt Enable Register
	0x0013 Hardware Interrupt Output Enable Register
	0x0016 RT Interrupt Output Enable Register
	0x0017 RT Configuration Register
	0x0019 RT Descriptor Table Base Address Register
	0x001C RT Bus A Select Register
	0x001D RT Bus B Select Register
	0x001F RT Alternate BIT Word Register
	0x004A RT Time Tag Utility Register
	0x0200 through 0x02FF: RT Illegalization Table
	0x0400 through 0x05FF: RT Descriptor Table

To manually start the RT after soft reset completion (indicated by READY signal assertion), the host must set RTSTEX bit 4 in the Master Configuration Register (0x0000) unless RT auto-start is enabled and auto-initialization feature is used.

MIL-STD-1760 Startup

A MIL-STD-1760 RT must be able to respond on the bus within 150ms following power turn-on. Between power-on and 150ms, it is acceptable for the RT to respond with the "Busy" bit set in the RT Status Word. The Mamba family RTs include a new feature to allow the RT to boot up in MIL-STD-1760 mode. In order to engage 1760 mode, the pin MODE1760 is asserted during a hardware reset. The pin status will be latched 200ns after the rising edge of Master Reset (the same time as the RT address). During 1760 mode, the device will respond to any valid command (with matching RT address) with the BUSY bit set in the status word. No data words will be transmitted and no interrupts or logging of data will occur. Mode 1760 operation may be confirmed by the host by reading Mode 1760 Status bit 7 in "Master Configuration Register 2 (0x004E)".

Interrupts

The Mamba and HI-6130/31 family of devices introduced some improvements and flexibility to interrupt management. The Mamba Family Remote Terminal Interrupts are controlled by two register triplets. One 3-register set is for hardware and the other is for the Remote Terminal itself. Each Register Triplet consists of an interrupt enable register, an interrupt output enable register, and a pending interrupt status register.

Using these registers, it is possible for the user to setup multiple levels of interrupt priority, whereby high priority interrupts will generate a hardware IRQ and lower priority interrupts will not generate the IRQ, but will still set bits in the appropriate pending interrupt register which may be polled. Interrupt options for RT Subaddress and mode codes is unchanged between HI-6120/21 and Mamba Family Devices.

The Mamba Family Remote Terminal also supports the use of the Interrupt Log Buffer. The size however was increased to now allow 32 entries each consisting of two 16-bit words that give the user information about the interrupt as well as a chronological history of interrupt events.

SPI Host Interface

The Mamba Family has introduced some improvements to the SPI host interface. The most visible improvement is that the maximum SPI clock frequency can operate up to 40MHz. In general, the SPI commands are identical between the HI-6121 and the MAMBA family. However, there are some differences. Fast access write commands which allow the application developer to directly address and quickly write registers 0-63 have been added.

Fast Access Write Commands for Registers 0-63

The 8-bit pattern for these write commands has the general form

1-0-R-R-R-R-R-R

where RRRRRR is the 6-bit register address. This format is slightly different than HI-6121 which has the following bit pattern to write registers 0-15:

1-0-R-R-R-R-0-0

Where RRRR is the 4-bit register address.

Memory Address Pointer Registers

Another notable change between HI-6121 and MAMBA is the inclusion of multiple Memory Address Pointer Registers. Whereas the HI-6121 only had a single MAP register, the Mamba Family of terminals now have 4 MAP registers.

The four memory address pointer registers are:

MAP1 Memory Address Pointer Register 0x000B
MAP2 Memory Address Pointer Register 0x000C
MAP3 Memory Address Pointer Register 0x000D
MAP4 Memory Address Pointer Register 0x000E

Each of these registers has a unique SPI op code that reads the MAP value in the register, and another op code that writes a new MAP value into the register. See SPI op code table in the respective datasheet. The host selects the active MAP register by writing the MAPSEL (memory address pointer select) bits 11-10 in the “Master Configuration Register 1 (0x0000)”, or by using the four defined “MAP Select” SPI op codes. The active MAP register contains the memory address used for indirect SPI read write access to registers and RAM.

SPI Command Summary

Differences are Highlighted in light green with **bold text**.

Table 5 - SPI Command Comparison

HI-6121			Mamba HI-6135/6/7/8
Hex Byte	**Read or Write**	**Description**	**Hex Byte**
Select / Enable a Memory Address Pointer			
N/A	**-------**	**Enable Memory Address Pointer at register 0x000B**	**0xD8**
N/A	**-------**	**Enable Memory Address Pointer at register 0x000C**	**0xD9**
N/A	**-------**	**Enable Memory Address Pointer at register 0x000D**	**0xDA**
N/A	**-------**	**Enable Memory Address Pointer at register 0x000E**	**0xDB**
Address Pointer Operations (no data is written or read, no pointer auto-increment)			
0xD0	-------	Add 1 to the current address pointer value in address pointer register	0xD0
0xD8	**-------**	**Add 2 to the current address pointer value in address pointer register**	**0xD2**
0xE0	**-------**	**Add 4 to the current address pointer value in address pointer register**	**0xD4**
Read/Write RAM or Register Location Using Current Address Pointer Value			
0x40	R	Read location addressed by current address pointer value	0x40
0xC0	W	Write location addressed by current address pointer value	0xC0
Increment Address Pointer Then Read/Write Addressed RAM or Register Location			
0x48	**R**	**Read addressed location after incrementing pointer**	**N/A**
0xC8	W	Write addressed location after incrementing pointer	0xC8
Special Purpose Commands			
0x50	**R**	**Copy RT Current Control Word address to Memory Address Pointer, then read the location addressed by the new pointer value (read the current Control Word)**	**0x48**
0x68	R	Add 0 to current Memory Address Pointer Value. Then …	0x68
0x70	R	Add 1 to current Memory Address Pointer Value. Then …	0x70
0x78	R	Add 2 to current Memory Address Pointer Value. Then copy value from newly addressed location to memory address pointer then read newly addressed location.	0x78
0xE8	W	Add 0 to current Memory Address Pointer Value. Then …	0xE8
0xF0	W	Add 1 to current Memory Address Pointer Value. Then …	0xF0
0xF8	W	Add 2 to current Memory Address Pointer Value. Then copy value from newly addressed location to memory address pointer then write newly addressed location.	0xF8
0x60	R	Read then add 4 to the current value of the Memory Address Pointer.	0x60
0x58	R	Write storage address of last-written Interrupt Address Word to the Memory Address Pointer, then read the Interrupt Address Word from the Interrupt Log buffer. Decrement Memory Address Pointer after read operation	0x58

Additional Resources

Demonstration/Evaluation Boards

The ADK-6135 or ADK-6138 evaluation boards provide sample software and a complete development environment that allows users to configure the RT and service messages from the Mamba family RT. These development kits provide example code written in ANSI 'C' and example applications and configuration code as well as many useful data structures and #defines.

RT Configuration GUI

Holt offers a Graphical User Interface (GUI) program that runs on Windows OS. The program is a wizard that guides users through various configuration options. This includes everything needed to configure RT settings, Subaddresses, Mode Codes, Buffering Options, Legalization, and Interrupts. The GUI supports all versions of Holt MIL-STD-1553 Remote Terminals.

The GUI outputs 4 text files that can be cut and Pasted into ANSI 'C' software. The four output files include the following:

1. Register configuration with all required bits set or cleared as required.

2. Command Illegalization Table to define legal and illegal commands

3. Descriptor Table to define all user Data Buffering Options and Interrupt Conditions

4. A RAM Usage definition file that defines all user data buffers and their locations and size.

Documentation

1. HI-6135 Data sheet

2. ADK-6135/36/37/38 User's Guide