



ADK-1585 Quick Start Guide –  
HI-1585 Transceiver  
Demonstration Board

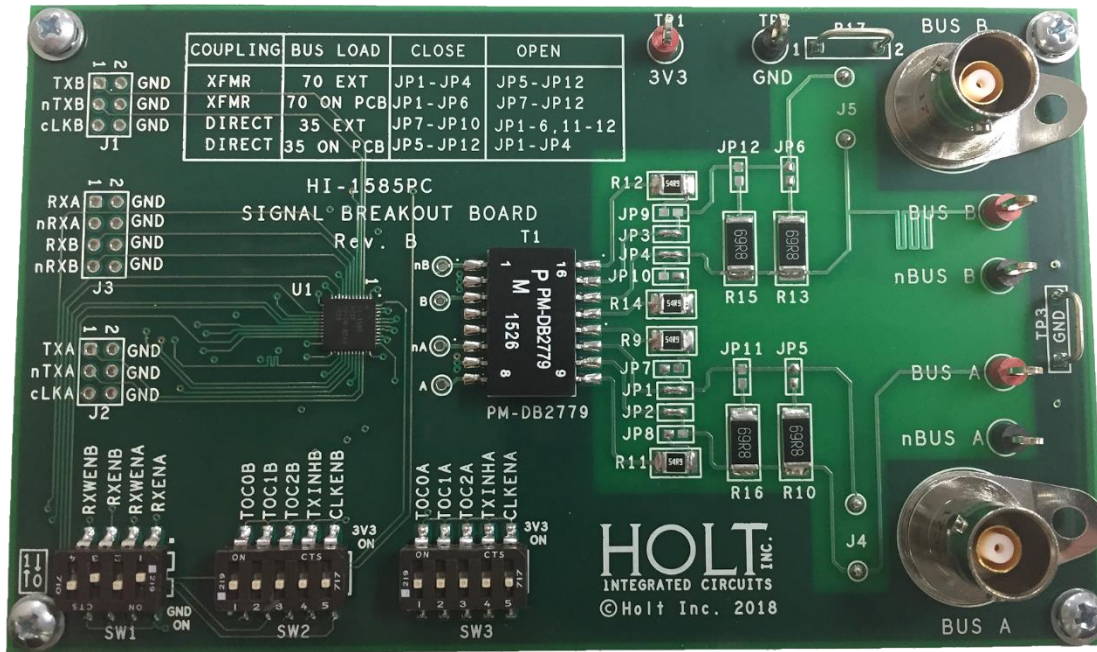
October 2018

**REVISION HISTORY**

<b>Revision</b>	<b>Date</b>	<b>Description of Change</b>
QSG-1585 Rev. New	03-06-17	Initial Release
Rev. A	10-05-18	Update board photo

## Introduction

The Holt HI-1585 is a MIL-STD-1553 transceiver with a unique range of hardware configuration options. The ADK-1585 Demo Board provides a convenient way to evaluate the various features.



HI-1585PC Signal Break-Out Board

## Set Up

To demonstrate the board, an external power supply providing 3.3VDC at 800mA is needed. Connect the power supply to test points 3V3 and GND along the top edge of the board.

## Bus Receive Signal Path

A pair of 3.3V CMOS logic-level outputs provides bipolar serial signals for connecting each bus to an external user-provided Manchester decoder. RXA and nRXA are the non-inverted and inverted receiver outputs for Bus A; RXB and nRXB are the receiver outputs for Bus B. The logic-level Bus A and Bus B receiver outputs can be enabled/disabled using the transceiver RXENA and RXENB inputs. On the HI-1585 Signal Break-Out Board, the receiver enable signals are controlled using DIP switches labeled RXENA and RXENB on switch package SW1. By default, receive signal pairs for both buses are enabled by these two SW1DIP switches set for logic-1.

The RX and nRX receive outputs have an option to stretch minimum output pulse width. When receiving differential signals near the MIL-STD-1553 minimum amplitude specification (860 mVpp or less when transformer-coupled), traditional transceivers produce narrow output pulses at RX and nRX because the

time that analog bus voltage exceeds the receiver threshold is much shorter than for a nominal or large amplitude bus voltage. Short HI-1585 RX and nRX receiver pulse outputs can optionally be stretched to have a minimum pulse width of 300ns. This function is enabled by strapping the ENPEXT configuration pin high. When ENPEXT is low, the comparator output is conventional.

For Bus A, ENPEXTA on the break-out board is controlled by the DIP switch labeled RXWENA on switch package SW1. For Bus B, ENPEXTB on the break-out board is controlled by the DIP switch labeled RXWENB on switch package SW1. *Note that receiver pulse stretching may cause issues with noise rejection, especially when noise pulses are stretched in the intermessage gap just before or during command sync rising edge. For this reason, receiver pulse width stretching is not recommended.*

The HI-1585 has weak pull-up resistors on ENPEXTA and ENPEXTB inputs. By default, the RXWENA and RXWENB DIP switches on package SW1 are set for logic-0 state, so neither bus has this option enabled on the HI-1585 Signal Break-Out Board.

### Bus Transmit Signal Path

A pair of 3.3V CMOS logic-level inputs accepts bipolar serial signals for driving each bus from an external user-provided Manchester encoder. Transmit for each bus can be enabled or inhibited using the corresponding TXINH transmit inhibit signal. For Bus A, the DIP switch labeled TXINHA on package SW3 controls transmit inhibit. For Bus B, the DIP switch labeled TXINHB on package SW2 controls transmit inhibit. By default, neither bus has transmit inhibited on the HI-1585 signal break-out board.

The transmit signal path for each bus includes the bipolar TX and nTX signals generated by the external Manchester encoder. Signal quality concerns dictate that the TX/nTX signals for each bus have matched characteristics. This includes matched conductor length and impedance, matched layer-to-layer vias (or even better, no vias). It is not always possible to achieve good matching on the board layout. The result: TX and nTX switching transitions are not quite simultaneous; the TX/nTX crossover occurs early or late. Crossover should occur mid-way between ground and the 3.3V supply rail to assure acceptable “output symmetry” or “tail-off” occurring at the end of long transmit messages. This effect is discussed at length in Holt application note AN-550.

### Transmit Signal Sync Option

To accurately synchronize TX and nTX inputs, the HI-1585 offers the option to simultaneously clock transmit input signals for each bus with a clock pulse input pin. When high, the ENCLKA input enables synchronized TX and nTX inputs for bus A. The DIP switch labeled CLKENA on switch package SW3 controls ENCLKA.

With synchronization enabled (ENCLKA = 1), the CLKA input pin synchronizes TXA and nTXA for bus A transmit. If using an FPGA encoder, the user must provide a brief positive clock pulse every time the TXA and nTXA signals change state. Logic levels present at the TXA and nTXA inputs are latched by CLKA rising edge. If ENCLKA is held low, the clocked input latches are bypassed and the CLKA input has no effect.

Similarly, the DIP switch labeled CLKENB on switch package SW2 controls ENCLKB to enable or disable synchronized operation for bus B, accomplished using the TXB, nTXB and CLKB inputs. The ENCLKA and ENCLKB input pins have weak pull-down resistors.

### Bus Tail-Off Trim

On DIP switch package SW3, switches labeled TOC0A, TOC1A and TOC2A are used in combination to provide up to +75mV or -75mV DC tail-off adjustment on Bus A, to compensate for a board layout deficiency that causes chronic, consistent tail-off which would benefit from an across-the-board fixed amplitude adjustment. The TOC switch settings select one of six correction levels. There are two “no correction” TOC combinations. Table 2 on page 6 in the HI-1585 data sheet summarizes the TOC switch combinations. Figures 3 and 4 in the data sheet show examples of various applied correction levels.

Tail-off trim for Bus B works similarly using switches labeled TOC0B, TOC1B and TOC2B on DIP switch package SW2. All TOC input pins have weak pull-down resistors that present logic-0 when the corresponding DIP switches are open.

### Flexible Bus Interface Configuration

The HI-1585 Signal Break-Out Board has several options for configuring both MIL-STD-1553 bus interfaces. The options are listed here and then fully described below:

- Direct-coupled or transformer-coupled bus interface
- On-board resistive dummy bus load or off-board conventional bus connection
- Optional ground connections for negative side of Buses A and B so that single conventional oscilloscope probes conveniently provide differential “Bus-Positive minus Bus-Negative” signal viewing.

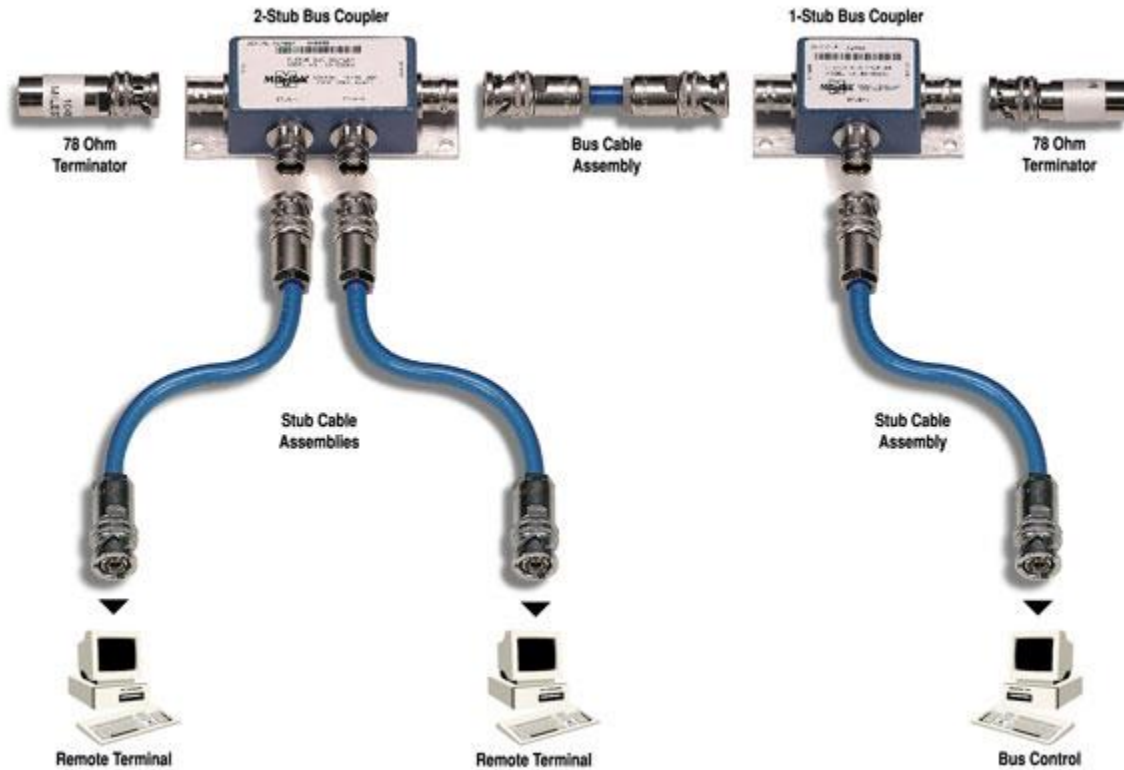
### Direct- or Transformer-Coupled Operation

The HI-1585 Signal Break-Out Board provides 12 solder jumpers for selecting direct- or transformer-coupled operation.

Direct-coupled 1553 bus interface is also known as a “short stub” connection because the terminal’s stub cable cannot exceed 12 inches (31 mm) in length. Direct-coupled bus interface requires a pair of current-limiting resistors in series with the bus connection. When configuration jumpers are set for direct-coupled operation, current-limiting resistors are provided on the break-out board.

## QSG-1585

Transformer-coupled 1553 bus interface is the predominant configuration used for terminal connection. This diagram shows a network comprised of three transformer-coupled terminals: a Bus Controller (BC) and two Remote Terminals (RTs). Stub cables must be < 20 feet (6.1 meters).



The HI-1585 Signal Break-Out Board (and user-provided protocol logic) takes the place of the BC or one of the RTs in the above diagram.

As seen above, each terminal's stub cable connects to the 1553 bus through a "bus coupler," which is typically an off-the-shelf hardware component comprised of coupling transformer(s) for one or more terminal stubs (each with its own pair of internal current-limiting resistors). Two bus couplers are shown above. The bus couplers have a bus connection jack at each end for serial connection into the 1553 bus structure. Each end of the bus has a 78Ω terminator. Holt application note AN-550 provides additional information about the direct- and transformer-coupled configurations.

### Dummy Resistor Bus Load Option

The HI-1585 Signal Break-Out Board provides 12 solder jumper locations for selection of direct- or transformer-coupled operation. The jumpers also select on-board resistor dummy bus load or off-board conventional 1553 bus connection, shown above. When enabled, the on-board dummy load replaces the stub cable assembly in the diagram and everything above it; the resistor load appears directly at the terminal bus interface. The load is 70Ω for transformer-coupled operation, or 35Ω for direct-coupled operation (using two parallel 70Ω resistors).

The twelve configuration jumpers are designated JP1 – JP12. A connection table printed on the HI-1585 signal break-out board tells you which jumpers to open and which to close for the four combinations of direct- vs. transformer-coupled operation and on-board dummy bus load vs. external conventional 1553 bus connection.

### **Single Scope Probe “Faux Differential” Viewing Option**

When characterizing a 1553 terminal, most bus measurements are the differential line-to-line stub voltage measured across the bus side of the terminal’s isolation transformer. For the HI-1585 signal break-out board, the transformer is the PM-DB2779 rectangular black cube, and the red and black differential test point pairs are labeled BUSA/nBUSA and BUSB/nBUSB for the two buses.

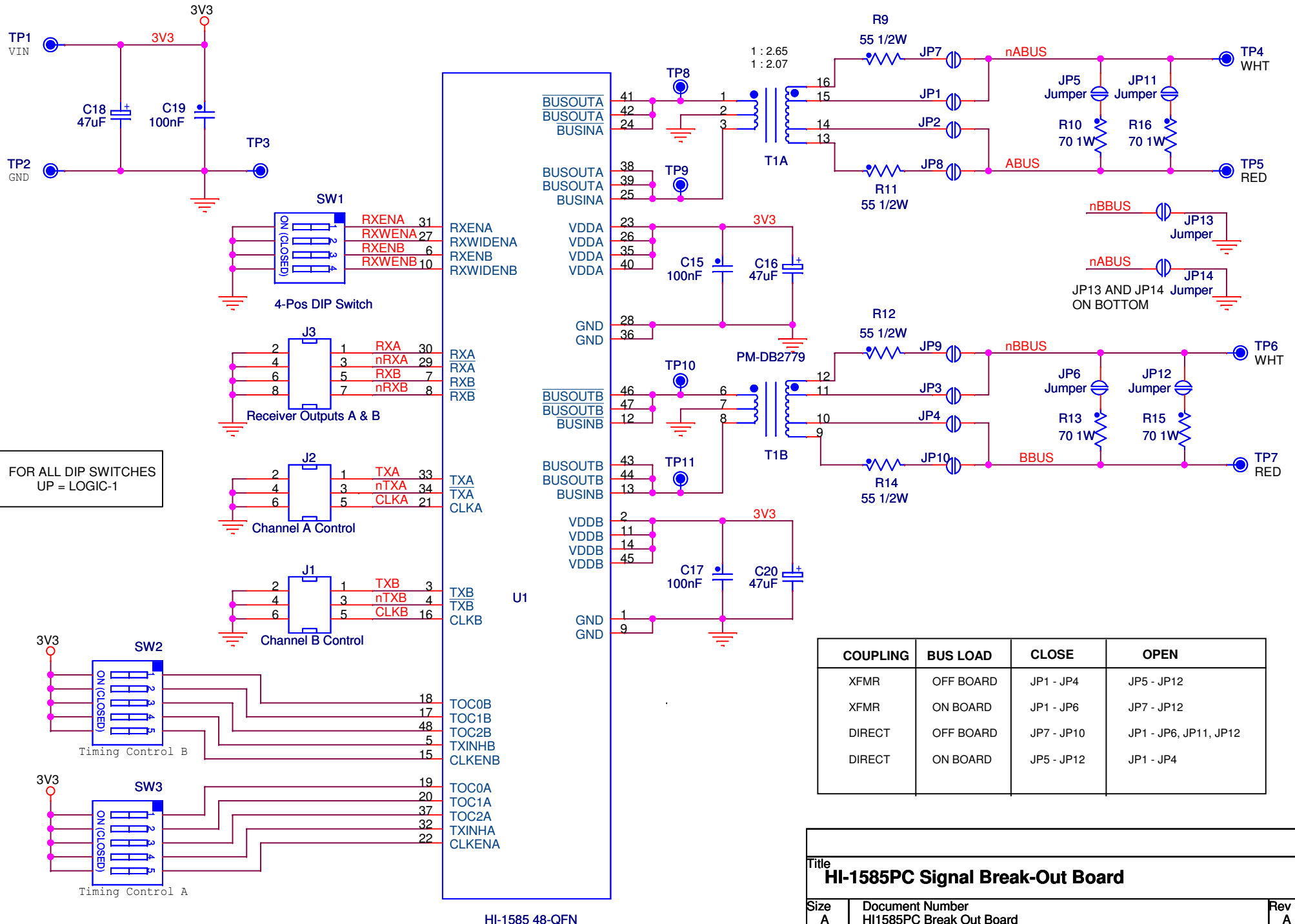
Differential line-to-line voltage measurement for Bus A can be accomplished by connecting oscilloscope probes for channel 1 and channel 2 to the BUSA and nBUSA test points respectively, and using scope built-in math function to observe “channel 1 minus channel 2”. Back-side solder jumpers JP13 and JP14 must be “open circuit” for this configuration.

If back-side solder jumpers JP13 (Bus B) and JP14 (Bus A) are closed, the minus side of buses A and B are grounded. The user can forgo the channel 2 oscilloscope connection to nBUSA; the single channel 1 probe connection to BUSA provides true differential viewing of Bus A stub voltage. This is strictly a convenience measure to be used when evaluating HI-1585 transceiver performance; the minus side of the 1553 bus stub would never be left grounded under normal circumstances for production hardware.

The above comments for configuring Bus A also apply for Bus B, substituting test points BUSB and nBUSB for test points BUSA and nBUSA respectively.

### **Board Schematic Diagram**

The schematic diagram for the HI-1585 Signal Break-Out Board is on the following page.



COUPLING	BUS LOAD	CLOSE	OPEN
XFMR	OFF BOARD	JP1 - JP4	JP5 - JP12
XFMR	ON BOARD	JP1 - JP6	JP7 - JP12
DIRECT	OFF BOARD	JP7 - JP10	JP1 - JP6, JP11, JP12
DIRECT	ON BOARD	JP5 - JP12	JP1 - JP4

Title <b>HI-1585PC Signal Break-Out Board</b>		
Size A	Document Number HI1585PC Break Out Board	Rev A
Date:	Tuesday, February 28, 2017	Sheet 1 of 1

HI-1585 48-QFN



<i>Item</i>	<i>Qty</i>	<i>Description</i>	<i>Reference</i>	<i>DigiKey</i>	<i>Mfr P/N</i>
1	1	PCB, Bare, Eval Board	N/A	-----	Jet Tech # 39192
2	3	Capacitor, Cer 0.1uF 20% 50V Z5U 0805	C15,C17,C19	399-1176-1-ND	Kemet C0805C104M5UACTU
3	3	Capacitor, 47uF 20% 16V Tant SMD 6032	C16,C18,C20	399-9739-1-ND	Kemet T491C476M016AT
4	4	Resistor, 54.9, 1% 1/2W 1210	R9,R11,R12,R14	P54.9AACT-ND	Panasonic ERJ-14NF54R9U
5	4	Resistor, 69.8, 1% 1W 2512	R10,R13,R15,R16	RHM69.8BBCT-ND	Rohm MCR100JZHF69R8
6	2	Header, Male 2x3 0.1" Pitch	J1,J2	S2012E-035-ND	Sullins EC03DAAN
7	1	Header, Male 2x4 0.1" Pitch	J3	S2012E-04-ND	Sullins PEC04DAAN
8	1	DIP Switch 4-Position SMD	SW1	CT2194MST-ND	CTS 219-4MST
9	2	DIP Switch 5-Position SMD	SW2,SW3	CT2195MST-ND	CTS 219-5MST
10	3	Test Point, Red Insulator, 0.062" hole	(+)BusA, (+)BusB, 3V3	36-5010-ND	Keystone 5010
11	2	Solid Bus Wire -20AWG - 1" Long	GND Test Loop	297 SV005-ND	Alpha Wire 297 SV005
12	2	Test Point, Black Insulator, 0.062" hole	(-)BusA, (-)BusB	36-5011-ND	Keystone 5011
13	1	IC HI-1585 48-QFN	U1	HOLT IC	Holt IC
14	1	Isolation Transformer PM-DB2779	T1	HOLT IC	Holt-Premier Magnetics
15	5	Rubber Foot, Bumpon Black Hemisphere, .312 X.200 H	Four corners and center	SJ5746-0-ND	3M SJ61A1