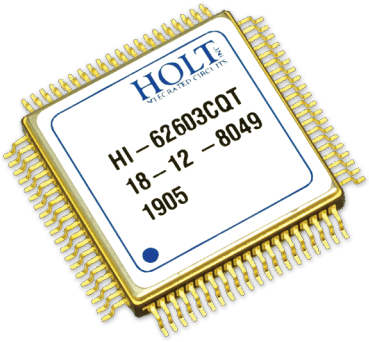
HOLT INTEGRATED CIRCUITS INC.

HI-6260

MIL-STD-1553
Simple System Remote Terminal (SSRT)

December 2019



1. Overview

The HI-6260CQ family is a fully integrated and dual redundant MIL-STD-1553 Simple System Remote Terminal (SSRT) solution which includes 1553 protocol and dual transceivers in a single package. The device is a direct pin compatible drop-in replacement for the Data Device Corporation (DDC®) Mini-ACE® Mark3 SSRT family of MIL-STD-1553 Terminals.

1.1. Simple System Remote Terminal (SSRT)

The SSRT provides a MIL-STD-1553 Remote Terminal interface for a simple system that doesn't have or usually require a microprocessor. It therefore provides a lower cost alternative to a traditional RT-only device with a microprocessor host interface. Communication is achieved via a DMA interface with a handshake data transfer mechanism. The device includes a 32-word deep FIFO for received messages and supports all MIL-STD-1553 message types, including mode codes. Any subset of the possible 1553 commands may be optionally illegalized by utilizing an illegalization table in an external RAM, or on a command-by-command basis by asserting the $\overline{\text{ILLEGAL}}$ input signal.

The RT will ignore invalid commands and only valid words will be stored in the FIFO. In addition, the device has a number of output signals which provide real-time status monitoring for events such as message errors, handshake failure, loopback test failure or transmitter timeout.

The RT address and parity are programmed directly via six input pins. An additional input signal is available to internally latch the RT address and an output signal is provided to indicate a parity error.

The SSRT provides an autonomous built-in self-test capability, which is automatically initiated following power turn-on or after the terminal has received an "Initiate Self-Test" mode command. The built-in self-test may be disabled via the auto-configuration feature, which also allows various other features to be enabled or disabled at start-up.

1.2. Features

- Fully Integrated Remote Terminal including dual 3.3V or 5V transceivers
- MIL-STD-1553A/B/1760 Compliant
- 32-Word Internal FIFO with burst mode capability
- 16-Bit DMA Interface
- External RT Address Inputs
- Built-in Self-Test
- Auto-Configuration Capability
- -40°C to +85°C or -55°C to +125°C
- 80-Pin Hermetic Gull Wing Package
  - 22.4mm x 22.4mm x 3.6mm

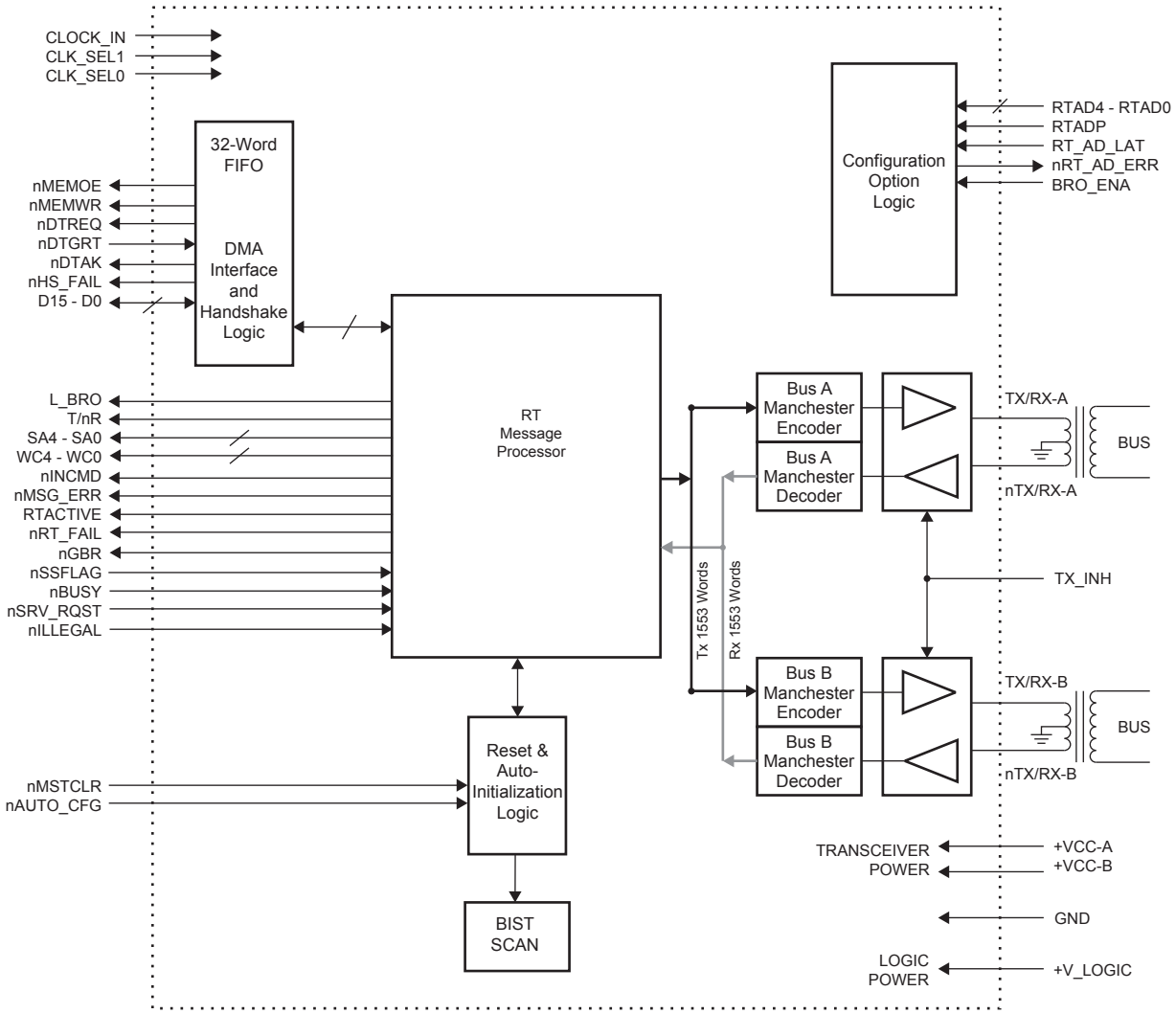
1.3. Application Benefits

- Simplified Board Design and Layout
- Third Party RT Validated
- Single Die for Improved Reliability
- Cost Effective Direct Drop-in Replacement for DDC® Mini-ACE® Mark3 SSRT Family

1.4. Cross Reference Guide

Holt P/N	DDC® P/N
HI-62605CQx	BU-64703G3-xxx
HI-62603CQx	BU-64703GC-xxx

1.5. Block Diagram



1.6. Loopback Test

The SSRT automatically performs a digital loopback self-test following every non-broadcast message and checks the message for validity. The internal receiver for the same bus is independent from the encoder logic used for bus transmission and the receiver detects and decodes the received replica of the transceiver's own transmission. The digital signal paths used for encoding and transmission (as well as reception and decoding) are fully tested without involving the external MIL-STD-1553 bus. If the loopback test fails, the Terminal Flag bit will be set in the SSRT status word for the next non-broadcast message.

1.7. Protocol Self-Test

The SSRT has the ability to perform a self-test of its internal protocol logic, including all registers and the internal FIFO. The test duration is about 32,000 clock cycles. During self-test, the SSRT will not respond to any messages received from the 1553 bus.

The protocol self-test may be run at power-up by asserting both the RSTBITEN input signal and Auto Configuration Parameter bit 5 to logic "1". The self-test will also be run if the device receives an Initiate Self-Test mode command from the 1553 bus.

If the protocol self-test fails, the Terminal Flag bit will be set in the SSRT status word. The BISTF, bit 8 in the BIST Word will also be set and the SSRT's $\overline{\text{RTFAIL}}$ output signal will be asserted to logic "0".

1.8. Built-In Self-Test (BIST) Word

The SSRT automatically populates a Built-In Self-Test Word, whose bits will read logic “1” to reflect errors flagged by the device. This word will be transmitted to the BC following a “Transmit BIT Word” mode command. The BIST word bit descriptions are provided below in Table 1.

Table 1. Internal Built-in Self Test (BIST) Word Definition

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	TXTO	R	0	Transmitter Timed Out. The transmitter timeout of 660.5µs was exceeded.
14	LBFB	R	0	Loopback Test Failure B. A loopback failure occurred on Bus B.
13	LBFA	R	0	Loopback Test Failure A. A loopback failure occurred on Bus A.
12	HSF	R	0	This bit will be set if the system fails to assert a Data Transfer Grant $\overline{\text{DTGRT}}$ within 10µs of the SSRT requesting a data transfer ($\overline{\text{DTREQ}}$ asserted).
11	TXSDB	R	0	Transmitter Shutdown B. A Transmitter Shutdown mode command was received on Bus A. This mode command shuts down the transmitter of the inactive bus.
10	TXSDA	R	0	Transmitter Shutdown A. A Transmitter Shutdown mode command was received on Bus B. This mode command shuts down the transmitter of the inactive bus.
9	TFINH	R	0	Terminal Flag Inhibited. An Inhibit Terminal Flag mode command was received.
8	BISTF	R	0	BIST Test Fail. The device failed its internal Built-In Self-Test routine.
7	DWCH	R	0	Data Word Count High. The number of data words received in the last message was higher than expected.
6	DWCL	R	0	Data Word Count Low. The number of data words received in the last message was lower than expected.
5	SNYCF	R	0	Incorrect Sync Received. A command sync bit was detected in a data word.
4	INVW	R	0	Invalid Word Received

Bit No.	Mnemonic	R/W	Reset	Bit Description
3	RTRTE	R	0	RT−to−RT Gap / Sync / Address Error. If the device is the receiving RT in an RT-to-RT transfer, this bit will be set if there is a gap time error (gap less than 2µs), incorrect sync or format error, or incorrect RT address.
2	RTRTTO	R	0	RT−to−RT Timeout Error. This bit will be set if the allowed RT-to-RT response time of about 17µs is exceeded.
1	RTRTCWE	R	0	RT−to−RT Command Word Error . If the device is the receiving RT in an RT-to-RT transfer, this bit will be set if there is an error in the Transmit Command Word, e.g. T/$\overline{R}$ bit is not logic “1”.
0 (LSB)	RXCWE	R	0	Received Command Word Error. This bit will be set if there is an error in a received Command Word.

1.9. Auto-Configuration

Auto-Configuration is controlled using the $\overline{\text{AUTO\_CFG}}$ input signal and allows six optional features to be enabled or disabled. Enabling or disabling each feature is controlled by the Auto-Configuration Parameters described below in Table 2.

If $\overline{\text{AUTO\_CFG}}$ is connected to logic “1”, then the auto-configuration is disabled and the six configuration parameters will be their default values of logic “1”.

If $\overline{\text{AUTO\_CFG}}$ is connected to logic “0”, then the configuration parameters are transferred over the data lines D5-D0 using a DMA data transfer.

Table 2. Auto-Configuration Parameters

Bit No.	Mnemonic	R/W	Default	Bit Description
5	RTSTF	R/W	1	If RTSTF is logic “1” (default) then the RT will go online if the Built-In Self-Test fails. If RTSTF is logic “0”, then the RT will go online only if the Built-In Self-Test passes.
4	TFLBKF	R/W	1	If TFLBKF is logic “1” (default), then the Terminal Flag bit will be set in the SSRT status word for the next non-broadcast message. If TFLBKF is logic “0”, then the Terminal Flag bit will not be set in the SSRT status word.
3	1553B	R/W	1	If 1553B is logic “1” (default), then the SSRT operates in MIL-STD-1553B mode. If 1553B is logic “0”, then the SSRT operates in MIL-STD-1553A mode.
2	SUB30	R/W	1	If SUB30 is logic “1” (default), then all data words for a receive command to subaddress 30 will be stored in the internal FIFO and not transferred to the external system. When a transmit command is subsequently received for subaddress 30, the data words will be read directly from the FIFO, instead of the external system. If SUB30 is logic “0”, then all data words for a receive command to subaddress 30 will be transferred to the external system.
1	BURST	R/W	1	If BURST is logic “1” (default), then Burst Mode is enabled. In Burst Mode, for a receive message, all received data words will be first stored in the internal FIFO and sent to the external system contiguously following reception of the last data word. If BURST is logic “0”, Burst Mode is disabled. Each received data word is transferred to the external system as it is received, requiring a DMA handshake for each data word.
0 (LSB)	BIST	R/W	1	If both the RSTBITEN input signal and the BIST parameter are logic “1” (default), then the SSRT will run the Built-In Self-Test on power-up following the rising edge of MSTCLR. If etiher RSTBITEN or BIST are logic “0”, then Built-In Self-Test is disabled.

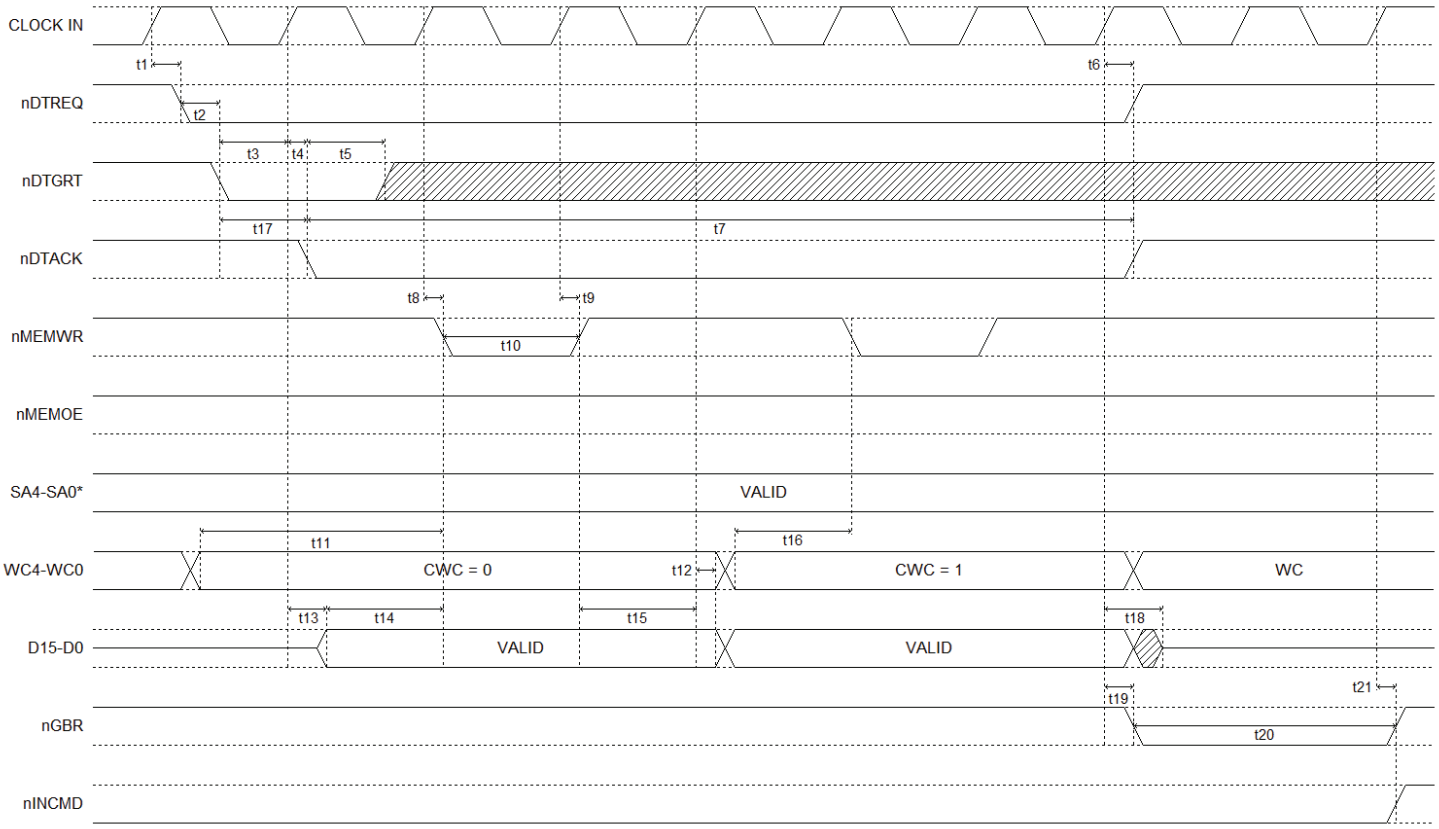
1.10. Clock Input

The supported clock frequencies are selected by the input signals CLK_SEL_1 and CLK_SEL_0, as shown in Table 3.

Table 3. Clock Frequency Selection

CLK_SEL_1	CLK_SEL_0	Clock Frequency
0	0	10 MHz
0	1	20 MHz
1	0	12 MHz
1	1	16 MHz

2. Timing Diagrams



NOTE: * L_BRO and T/$\overline{R}$ show the same waveform.

Figure 1. DMA Write Transfer (Burst Mode) Timing for Two Data Words

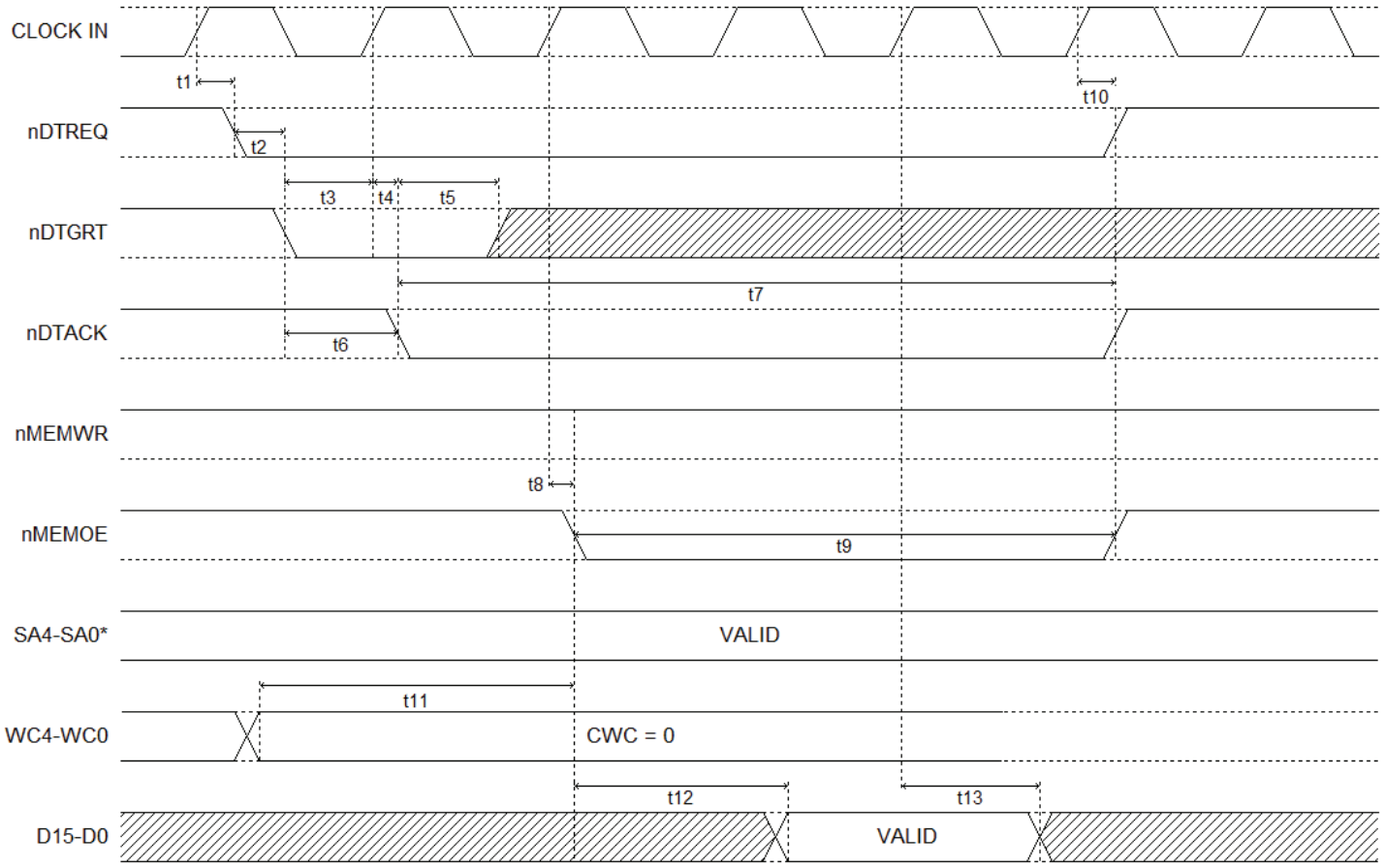
Timing Diagrams

Table 4. DMA Write (Burst Mode) Timing for two data words

Time	Description	Clock Frequency	Response @ 5V			Response @ 3.3V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t1	CLOCK IN rising edge to $\overline{\text{DTREQ}}$ falling edge	All			40			40	ns
t2	$\overline{\text{DTREQ}}$ falling edge to $\overline{\text{DTGRT}}$ falling edge	All			10			10	µs
t3	$\overline{\text{DTGRT}}$ low setup time to CLOCK IN rising edge	All	10			15			ns
t4	CLOCK IN rising edge to $\overline{\text{DTACK}}$ falling edge	All			40			40	ns
t5	$\overline{\text{DTGRT}}$ hold time from $\overline{\text{DTACK}}$ falling edge	All			30			30	ns
t6	CLOCK IN rising edge to $\overline{\text{DTREQ}}$ and $\overline{\text{DTACK}}$ rising edge	All			30			40	ns
t7	$\overline{\text{DTACK}}$ low pulse width	20 MHz	290	300		290	300		ns
		16 MHz	365	375		365	375		ns
		12 MHz	490	500		490	500		ns
		10 MHz	590	600		590	600		ns
t8	CLOCK IN rising edge to $\overline{\text{MEMWR}}$ falling edge	All			40			40	ns
t9	CLOCK IN rising edge to $\overline{\text{MEMWR}}$ rising edge	All			30			40	ns
t10	$\overline{\text{MEMWR}}$ low pulse width	20 MHz	40	50		40	50		ns
		16 MHz	52.5	62.5		52.5	62.5		ns
		12 MHz	73.3	83.3		73.3	83.3		ns
		10 MHz	90	100		90	100		ns
t11	CWC setup time to $\overline{\text{MEMWR}}$ falling edge (first word only)	20 MHz	60			60			ns
		16 MHz	85			85			ns
		12 MHz	127			127			ns
		10 MHz	160			160			ns
t12	Data output hold time from CLOCK IN rising edge	All	10			15			ns
t13	CLOCK IN rising edge delay to output data valid	All			40			40	ns
t14	Data output setup time to $\overline{\text{MEMWR}}$ falling edge	20 MHz	10			10			ns
		16 MHz	22			22			ns
		12 MHz	43			43			ns
		10 MHz	60			60			ns

Time	Description	Clock Frequency	Response @ 5V			Response @ 3.3V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t15	Data output and CWC hold time from $\overline{\text{MEMWR}}$ rising edge	20 MHz	20			10			ns
		16 MHz	33			23			ns
		12 MHz	53			43			ns
		10 MHz	70			60			ns
t16	CWC setup time to $\overline{\text{MEMWR}}$ falling edge (except first word)	20 MHz	10			10			ns
		16 MHz	23			23			ns
		12 MHz	43			43			ns
		10 MHz	60			60			ns
t17	$\overline{\text{DTGRT}}$ falling edge to $\overline{\text{DTACK}}$ falling edge	20 MHz			100			105	ns
		16 MHz			113			118	ns
		12 MHz			133			138	ns
		10 MHz			150			155	ns
t18	CLOCK IN rising edge delay to output data tri-state	All			40			40	ns
t19	CLOCK IN rising edge to $\overline{\text{GBR}}$ falling edge	All			40			40	ns
t20	$\overline{\text{GBR}}$ low pulse width	20 MHz	90	100		90	100		ns
		16 MHz	115	125		115	125		ns
		12 MHz	157	167		157	167		ns
		10 MHz	190	200		190	200		ns
t21	$\overline{\text{INCMD}}$ rising edge from CLOCK IN rising edge	All			30			40	ns

Timing Diagrams



NOTE: * L_BRO and T/$\overline{R}$ show the same waveform.

Figure 2. DMA Read Transfer Timing (Single Word)

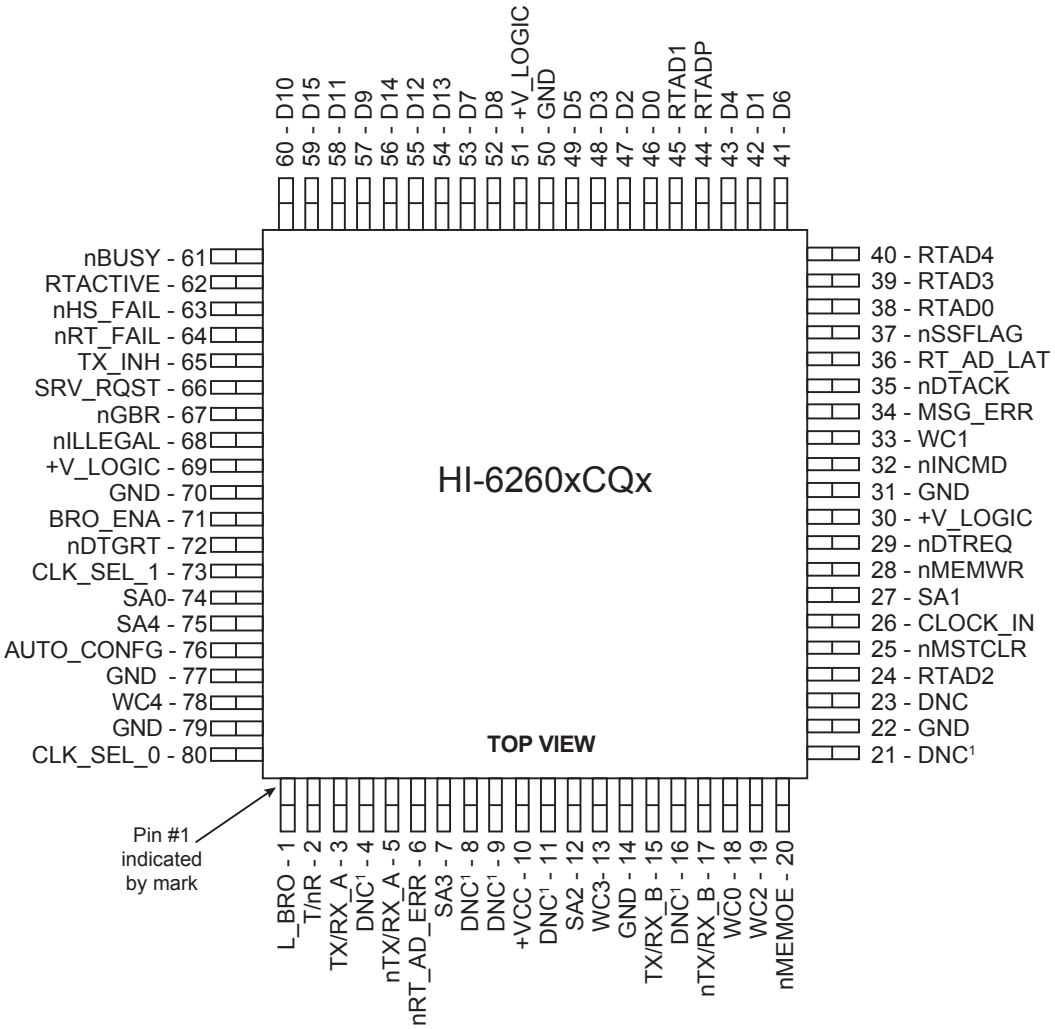
Table 5. DMA Read Transfer Timing

Time	Description	Clock Frequency	Response @ 5V			Response @ 3.3V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t1	CLOCK IN rising edge to $\overline{\text{DTREQ}}$ falling edge	All			40			40	ns
t2	$\overline{\text{DTREQ}}$ falling edge to $\overline{\text{DTGRT}}$ falling edge	All			10			10	µs
t3	$\overline{\text{DTGRT}}$ low setup time to CLOCK IN rising edge	All			10			10	ns
t4	CLOCK IN rising edge to $\overline{\text{DTACK}}$ falling edge	All			40			40	ns
t5	$\overline{\text{DTGRT}}$ hold time from $\overline{\text{DTACK}}$ falling edge	All			30			30	ns
t6	$\overline{\text{DTGRT}}$ falling edge to $\overline{\text{DTACK}}$ falling edge	20 MHz			100			105	ns
		16 MHz			113			118	ns
		12 MHz			133			138	ns
		10 MHz			150			155	ns
t7	$\overline{\text{DTACK}}$ low pulse width	20 MHz		200			200		ns
		16 MHz		250			250		ns
		12 MHz		333			333		ns
		10 MHz		400			400		ns
t8	CLOCK IN rising edge to $\overline{\text{MEMOE}}$ falling edge	All			40			40	ns
t9	$\overline{\text{MEMOE}}$ low pulse width	20 MHz		150			150		ns
		16 MHz		188			188		ns
		12 MHz		250			250		ns
		10 MHz		300			300		ns
t10	CLOCK IN rising edge to $\overline{\text{DTREQ}}$, $\overline{\text{DTACK}}$ and $\overline{\text{MEMOE}}$ rising edge	All			30			40	ns
t11	CWC setup time to $\overline{\text{MEMOE}}$ falling edge	20 MHz	60			60			ns
		16 MHz	85			85			ns
		12 MHz	127			127			ns
		10 MHz	160			160			ns
t12	Input data valid delay from falling edge of $\overline{\text{MEMOE}}$	20 MHz			80			70	ns
		16 MHz			105			95	ns
		12 MHz			146			136	ns
		10 MHz			180			170	ns

Timing Diagrams

Time	Description	Clock Frequency	Response @ 5V			Response @ 3.3V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t13	Data input hold time from CLOCK IN rising edge	All	30			30			ns

3. Pin Diagrams



Notes:
1. Do Not Connect (Factory test pin).
2. Prefix “n” denotes an inverted or negative signal, e.g. nMSTCLR = $\overline{\text{MSTCLR}}$, etc.

Figure 3. HI-6260xCQx Gull Wing Package Pinouts

4. Pin Descriptions

Table 6. Power and Ground

Signal Name	Function	Description
+VCC	Power Supply	3.3V or 5.0V DC power supply for transceiver. 3.3V for HI-62603CQxx. 5.0V for HI-62605CQxx.
+V_LOGIC	Power Supply	DC power supply for digital logic. This pin supports both 3.3V or 5V logic supplies.
GND	Power Supply	Power supply ground.

Table 7. MIL-STD-1553 Isolation Transformer Connections

Signal Name	Function	Description
TX/RX-A	Analog I/O	Bi-directional Bus A interface to external MIL-STD-1553 isolation transformer. Observe positive / negative polarity.
$\overline{\text{TX/RX-A}}$	Analog I/O	
TX/RX-B	Analog I/O	Bi-directional Bus B interface to external MIL-STD-1553 isolation transformer. Observe positive / negative polarity.
$\overline{\text{TX/RX-B}}$	Analog I/O	

Table 8. Data and Command/Address Busses

Signal Name	Function	Description
D15 (MSB) − D0 (LSB)	Data inputs or Data outputs	Bi-directional data bus for host read/write operations on registers and RAM.
L_BRO	Digital Output	This output signal indicates receipt of a broadcast command (logic “1”). If a non-broadcast command is received, this signal will logic “0”.
T/$\overline{R}$	Digital Output	This output signal indicates if a received command is a transmit command (logic “1”) or a receive command (logic “0”).
SA4 − SA0	Digital Outputs	These 5 output signals indicate the value of the subaddress in the received command word. .
WC4 − WC0	Digital Outputs	Initially, when a new command word is received, output signals WC[4:0] will indicate the value of the Word Count or Mode Code field of the received command word. For Mode Code commands, the value of the mode code field will be latched until the next command word is received. For non-Mode Code commands, the WC[4:0] signals will be updated to reflect the current data word count as each data word is transferred to the system (receive command) or read from the system and transferred to the device (transmit command).

Table 9. DMA Interface Signals

Signal Name	Function	Description
$\overline{\text{DTREQ}}$	Digital Output	This active low output is a handshake signal used by the device to request access to the external data bus. The handshake is complete when the $\overline{\text{DTGRT}}$ input signal is asserted in response.
$\overline{\text{DTGRT}}$	Digital Input	This input signal completes the handshake following a $\overline{\text{DTREQ}}$ request and is asserted to indicate that control of the data bus has been released to the device.
$\overline{\text{DTACK}}$	Digital Output	This active low output is asserted to acknowledge a data transfer grant ($\overline{\text{DTGRT}}$) and indicates that the device has accepted control of the external data bus D[15:0].
$\overline{\text{HS\_FAIL}}$	Digital Output	Handshake Fail. This output signal will be asserted low when a $\overline{\text{DTGRT}}$ (Data Transfer Grant) signal is not received in time following a $\overline{\text{DTREQ}}$ (Data Transfer Request).
$\overline{\text{MEMOE}}$	Digital Output	This signal will be asserted low for three clock cycles as each data word is read from the external system.
$\overline{\text{MEMWR}}$	Digital Output	This signal will be asserted low during write cycles to the external system.

Table 10. RT Address

Signal Name	Function	Description
RTAD4 (MSB)	Digital Input	RT Address Input signals.
RTAD3	Digital Input	
RTAD2	Digital Input	
RTAD1	Digital Input	
RTAD0 (LSB)	Digital Input	
RTADP	Digital Input	Remote Terminal Address Parity. Used to provide odd parity for the RT address on RTAD[4:0].
RT_AD_LAT	Digital Input	RT Address Latch. This input signal is used to control how the RT address is latched internally. If RT_AD_LAT is logic “0”, then the RT address and parity will simply track RTAD4:0 and RTADP inputs. If RT_AD_LAT transitions from logic “0” to logic “1”, the values on RTAD4:0 and RTADP will be latched on the rising edge of RT_AD_LAT.
$\overline{\text{RT\_AD\_ERR}}$	Digital Output	If this output is logic “0”, it indicates the correct parity was not provided between RTAD[4:0] and RTADP inputs. If this output is logic “1”, correct (odd) parity was provided between RTAD[4:0] and RTADP inputs.

Table 11. RT Status Word Inputs

Signal Name	Function	Description
$\overline{\text{ILLEGAL}}$	Digital Input	Commands may be illegalized on an individual basis by asserting this input (logic “0”). In this case, the Message Error bit in the transmitted RT Status Word will be logic “1”. If this input is logic “1”, the Message Error bit in the transmitted RT Status Word will remain logic “0”.
$\overline{\text{SRV\_RQST}}$	Digital Input	If this input is logic “0”, the Service request bit in the transmitted RT Status Word will be logic “1”. If this input is logic “1”, the Service request bit in the transmitted RT Status Word will be logic “0”.
$\overline{\text{SSFLAG}}$	Digital Input	If asserted (logic “0”), the Subsystem Flag bit will be set in the transmitted RT Status Word.
$\overline{\text{BUSY}}$	Digital Input	If asserted (logic “0”), the Busy bit will be set to logic “1” in the transmitted RT Status Word.

Table 12. RT Status Signals

Signal Name	Function	Description
RTACTIVE	Digital Output	This output signal will be logic “1” when the RT is active and communicating with the MIL-STD-1553 bus. This signal will remain logic “0” while the RT is executing a built-in self test or during auto configuration.
$\overline{\text{INCMD}}$	Digital Output	$\overline{\text{INCMD}}$ is asserted low whenever a message is in progress.
$\overline{\text{GBR}}$	Digital Output	This output signal will be asserted low for two clock cycles whenever a valid command is received and transferred to the external system.
$\overline{\text{MSG\_ERR}}$	Digital Output	This output signal will be asserted low to indicate the RT detected a message error on the 1553 bus. $\overline{\text{MSG\_ERR}}$ will be cleared (logic “1”) when the next valid command is received or upon assertion of MSTCLR.
$\overline{\text{RT\_FAIL}}$	Digital Output	This output signal will be asserted low when the RT failed its built-in self-test.

Table 13. Reset and Control Inputs

<table>
<tr><th>Signal Name</th><th>Function</th><th colspan="3">Description</th></tr>
<tr><td>$\overline{\text{MSTCLR}}$</td><td>Digital Input</td><td colspan="3">Active low Reset input.</td></tr>
<tr><td>$\overline{\text{AUTO\_CFG}}$</td><td>Digital Input</td><td colspan="3">If this input is logic “0”, then auto configuration is enabled.
Auto configuration is performed following assertion of $\overline{\text{MSTCLR}}$ by a DMA read transfer over data bus inputs D[5:0].
If this input is logic “0”, then auto configuration is disabled.</td></tr>
<tr><td>BRO_ENA</td><td>Digital Input</td><td colspan="3">Broadcast Enable.
Setting this bit to logic “1” will enable broadcast commands, i.e. RT address 31 will be recognized as the broadcast subaddress.</td></tr>
<tr><td>TX_INH</td><td>Digital Input</td><td colspan="3">Setting this input to logic “1” will force both BUS A and BUS B transmitters to shutdown.</td></tr>
<tr><td rowspan="6">CLOCK_IN</td><td rowspan="6">Digital Input</td><td colspan="3">20 MHz, 16 MHz, 12 MHz, or 10 MHz clock input signal.
The frequency must be specified by the CLK_SEL_1 and CLK_SEL_0 inputs as follows:</td></tr>
<tr><th>CLK_SEL_1 Input</th><th>CLK_SEL_0 Input</th><th>Frequency</th></tr>
<tr><td>0</td><td>0</td><td>10 MHz</td></tr>
<tr><td>0</td><td>1</td><td>20 MHz</td></tr>
<tr><td>1</td><td>0</td><td>12 MHz</td></tr>
<tr><td>1</td><td>1</td><td>16 MHz</td></tr>
</table>

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Supply voltages	Logic +3.3V	-0.3 V to +6.0 V
	Transceivers +3.3V (not transmitting)	-0.3 V to +6.0 V
	Transceivers +3.3V (transmitting)	-0.3 V to +4.5 V
	Transceivers +5V	-0.3 V to +7.0 V
Logic input voltage range		-0.3 V to +6.0 V
Receiver differential voltage		10 Vp-p
Solder Temperature (reflow)		260ºC
Junction Temperature		175ºC
Storage Temperature		-65ºC to +150ºC

5.2. Recommended Operating Conditions

Parameters		Limits			Unit
		Min	Typ	Max	
Supply Voltages	Logic	3.0	3.3	3.6	V
	3.3V Transceivers	3.14	3.3	3.46	V
	5.0V Transceivers	4.75	5.0	5.25	V
Temperature Range	Industrial	-40		85	ºC
	Extended	-55		125	ºC

5.3. DC Electrical Characteristics

T_A = Operating Temperature Range

Parameters		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Power Supply							
Operating Supply Voltages	3.3V Logic	V_{Logic}		3.0	3.3	3.6	V
	3.3V Transceivers	V_{DD}		3.14	3.3	3.46	V
	5.0V Transceivers	V_{DD}		4.75	5.0	5.25	V
Power Supply Current See Note 1	V_{LOGIC} = 3.3V V_{DD} = 5.0V	I_{CC1}	Not Transmitting	-	-	15	mA
		I_{CC2}	Continuous supply current while one bus transmits @ 50% duty cycle, 70Ω resistive load	-	-	330	mA
		I_{CC23}	Continuous supply current while one bus transmits @ 100% duty cycle, 70Ω resistive load	-	-	565	mA
Power Dissipation See Note 2	V_{LOGIC} = 3.3V V_{DD} = 5.0V	PD_1	Not Transmitting	-	-	60	mW
		PD_2	Transmit one bus @ 50% duty cycle, 70Ω resistive load	-	-	1.05	W
		PD_3	Transmit one bus @ 100% duty cycle, 70Ω resistive load	-	-	1.55	W
Logic							
Input Voltage (High)		V_{IH}	All digital inputs, except CLK_{IN}	2.1	-	-	V
			CLK_{IN}	0.8			V_{DD}
Input Voltage (Low)		V_{IL}	All digital inputs, except CLK_{IN}	-	-	0.7	V
			CLK_{IN}			0.2	V_{DD}
Input Current (High)		I_{IH}	All digital inputs, except CLK_{IN}, V_{LOGIC} = 3.6V = V_{IH}	-10	-	-10	µA
			V_{LOGIC} = 3.6V, V_{IH} = 2.7V	-350	-	-33	µA
			CLK_{IN}	-10	-	10	µA
Input Current (Low)		I_{IL}	All digital inputs, except CLK_{IN}, V_{LOGIC} = 3.6V, V_{IL} = 0.4V	-350	-	-33	µA
			CLK_{IN}	-10	-	10	µA
Output Voltage (High)		V_{OH}	V_{LOGIC} = 3.0V, V_{IH} = 2.7V, V_{IL} = 0.2V, I_{OH} = max	2.4	-	-	V
Output Voltage (Low)		V_{OL}	V_{LOGIC} = 3.0V, V_{IH} = 2.7V, V_{IL} = 0.2V, I_{OL} = max	-	-	0.4	V
Output Current (High)		I_{OH}	V_{LOGIC} = 3.0V	-	-	-2.2	mA
Output Current (Low)		I_{OL}	V_{LOGIC} = 3.0V	2.2	-	-	mA

Parameters		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
RECEIVER (Measured at Point "AD" in Figure 6 unless otherwise specified)							
Input Resistance		R_{IN}	Differential	20	-	-	kΩ
Input Capacitance		C_{IN}	Differential	-	-	5	pF
Common Mode Rejection Ratio		CMRR		40	-	-	dB
Input Level		V_{IN}	Differential	-	-	9	Vp-p
Input Common Mode Voltage		V_{ICM}		-10	-	+10	V-pk
Threshold Voltage (Direct-Coupled)	Detect	V_{THD}	1 MHz Sine Wave (Measured at Point "AD" in Figure 6)	1.2	-	20.0	Vp-p
	No Detect	V_{THND}		-	-	0.28	Vp-p
Threshold Voltage (Transformer-Coupled)	Detect	V_{THD}	1 MHz Sine Wave (Measured at Point "AT" in Figure 7)	0.86	-	14.0	Vp-p
	No Detect	V_{THND}		-	-	0.2	Vp-p
TRANSMITTER (Measured at Point "AD" in Figure 6 unless otherwise specified)							
Output Voltage	Direct Coupled	V_{OUT}	35Ω Load	6.0	7.0	9.0	Vp-p
	Transformer Coupled	V_{OUT}	70Ω Load (Measured at Point "AT" in Figure 7)	20.0	22	27.0	Vp-p
Output Noise		V_{ON}	Differential, Direct Coupled	-	-	10.0	mVp-p
Output Dynamic Offset Voltage	Direct Coupled	V_{DYN}	35Ω Load	-90	-	90	mV
	Transformer Coupled	V_{DYN}	70Ω Load (Measured at Point "AT" in Figure 7)	-250	-	250	mVp
Rise/Fall Time		$t_{r/f}$	MIL-STD-1553B compliant	100	150	300	ns
Output Resistance		R_{OUT}	Differential, not transmitting	10	-	-	kΩ
Output Capacitance		C_{OUT}	1 MHz sine wave	-	-	15	pF
Clock Input							
Frequency	(Default)	CLK_{IN}			16.0		MHz
	(option)				12.0		MHz
	(option)				10.0		MHz
	(option)				20.0		MHz
MIL-STD-1553 Message Timing							
RT-to-RT Response Timeout (mid-parity to mid-sync)				17.5	18.5	19.5	µs
RT Response Time (mid-parity to mid-sync)				4		7	µs
Transmitter Watchdog Timeout					660.5		µs

Note 1: In actual use, the highest practical transmit duty cycle is 96%, occurring when a Remote Terminal responds to a series of 32 data word transmit commands (RT to BC) repeating with minimum intermessage gap of 4µs (2µs dead time) and typical RT response delay of 5µs.

Note 2: While one bus continuously transmits, the power delivered by the power supply is 5.0V × 565mA max = 2.825W. Of this, 1.55W is dissipated in the device, the remainder in the load.

5.4. MIL-STD-1553 Bus Interface

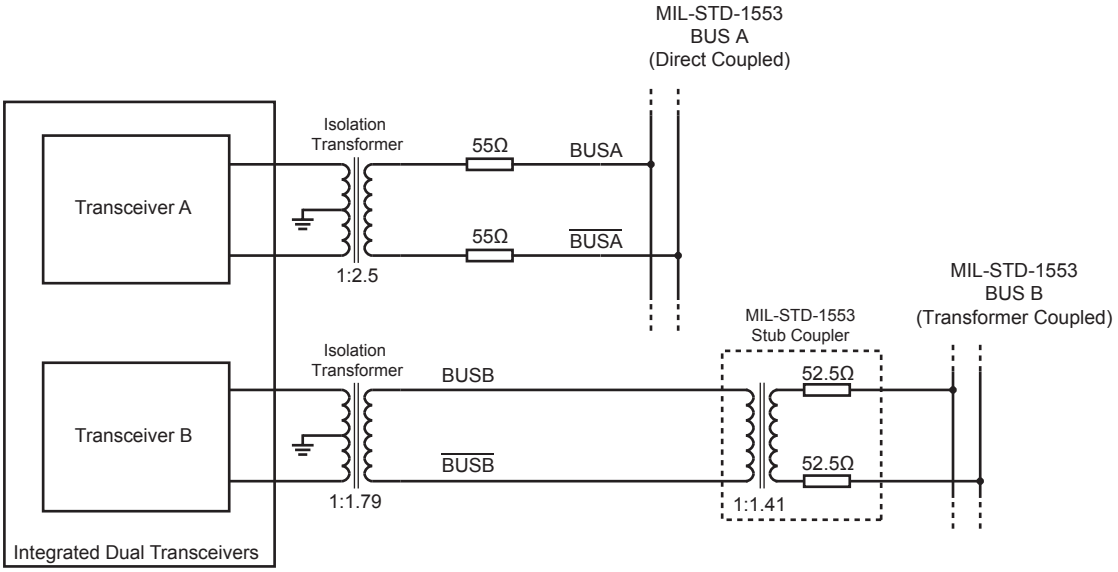


Figure 4. Bus Connection Example (HI-62605CQx, 5.0V transceivers)

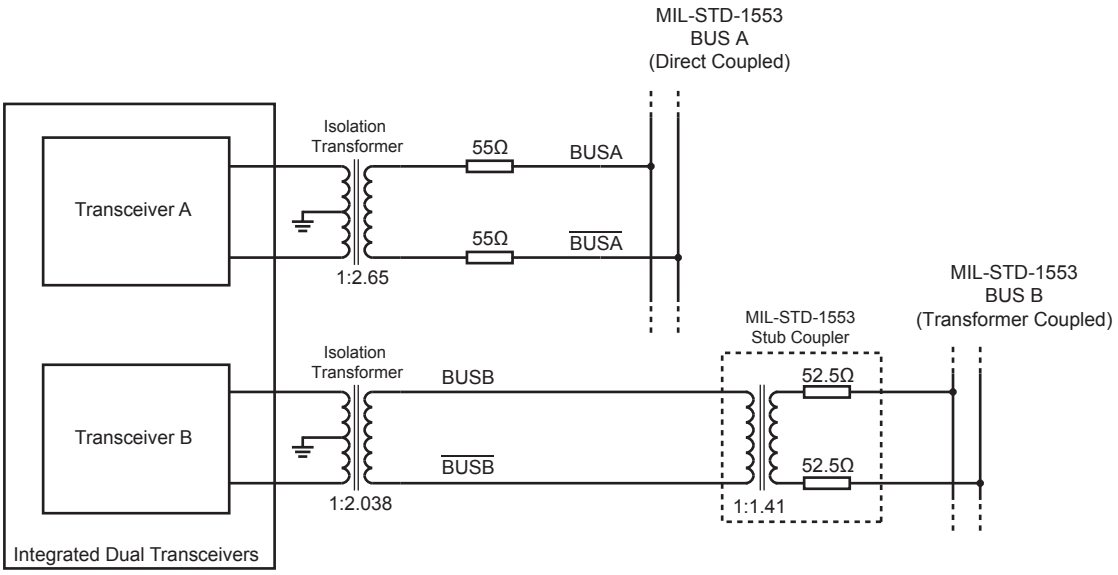


Figure 5. Bus Connection Example (HI-62603CQx, 3.3V transceivers)

5.5. MIL-STD-1553 Test Circuits

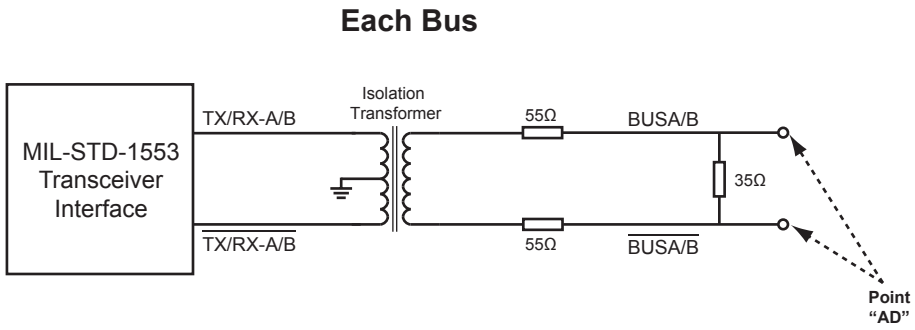


Figure 6. MIL-STD-1553 Direct Coupled Test Circuits

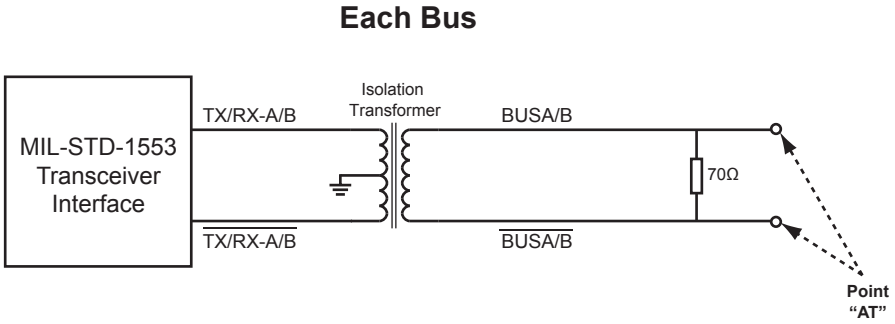


Figure 7. MIL-STD-1553 Transformer Coupled Test Circuits

6. Package Dimensions

Dimensions: inches (mm)

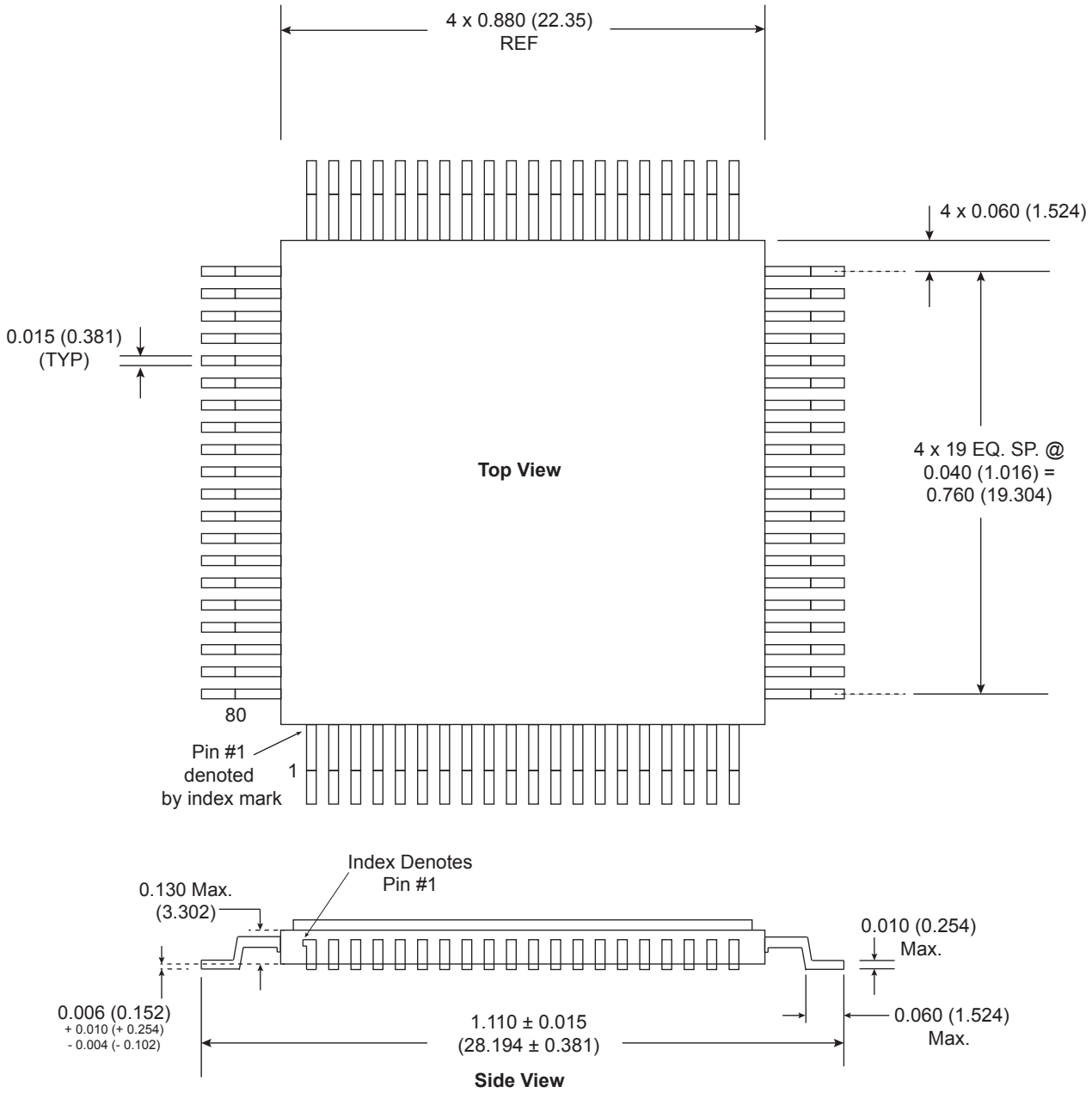


Figure 8. 80-Pin Gull Wing Package Dimensions

7. Ordering Information − 80 Pin Gull Wing Package

HI - 6260 x CQ x x

- Blank = Leaded, non-RoHS compliant[1]
- F = RoHS compliant

- I = −40°C to +85°C
- T = −55°C to +125°C
- M = −55°C to +125°C with burn-in
- R = Same as M, MIL-PRF compliant
- D = Same as R, with PIND testing

- CQ = Ceramic 80-pin gull wing package

- 3 = 3.3V Transceiver supply voltage
- 5 = 5.0V Transceiver supply voltage

- 6260 = RT only with simple system (no processor) interface (SSRT)

Note 1: Solder dipped, Sn/Pb solder

8. Revision History

Revision	Date	Description of Change
DS6260, Rev. New	05/23/18	Initial Release
Rev. A	05/23/19	Add package photo to title page. Add dimension units to package drawing.
Rev. B	12/20/19	Add more detail to block diagram. Add pin diagram and clarify pin descriptions. Other minor updates and corrections.